(handwritten annotations:) CATS 4 5 VAC   CB 5 12   22   DISH 24   27   35   P.PACK 42   CIRC   EPROM PROG 48 58 ERRORS   PROG 59 SERVICE   63 PREAMP.
(handwritten:) 9 NEW ADDRESS P.E. MAG   1 NOTE PRICES FOR OWN USE

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ideas, and all the latest product information from our advertisers.

THE SCIENCE MAGAZINE FOR SERIOUS ELECTRONICS ENTHUSIASTS

CATALOGUE CASEBOOK

We have recently received details of the following catalogues and literature:

Betronex are offering new colour technical liturature on their **EE Designer PCB CAD** system. **Betronex (UK) Ltd,** 1 Wells Yard, High Street, Ware, Herts, SG12 9AS.

Cricklewood Electronics. 'Crickles the Cat' looks out again from the cover of the **10th edition mid 1987 catalogue.** This well known cat offers hundreds of lower prices and new devices. **Cricklewood Electronics Ltd,** 40 Cricklewood Broadway, London NW2 3ET.

EOCS have sent their latest interesting and informative magazine. The Electronic Organ Constructors Society is **an organisation well worth joining** if you are interested in electronics and music. **ECOS,** 5 Gander Close, Hartcliffe, Bristol, BS13 9PN.

Lux-Therm Products announce their new catalogue describing high intensity **infrared heating modules** and tools. **Lux-Therm Products,** Unit M, Portway Industrial Estate, Andover, Hants, SP10 3LU.

M.S. Components. 1987 catalogue for **OEM and Industrial Electronics distribution,** incorporating the **Steatite Group** catalogue. **M.S. Components Ltd,** Zephyr House, Waring Street, West Norwood, London SE27 9LH.

Walmore Communicator. Reviews of fibre optic technology and components from **Walmore Electronics Ltd,** Laser House, 132-140 Goswell Road, London EC1B 1BX.

Half-Price Stripper

ELECTRONIC and Computer Workshop Ltd. (ECW) announces an extra special offer for the popular Bib No 9, professional-quality wire stripper. At less than half the recommended retail price, this is a unique opportunity to obtain a quality tool at an unrepeatable price, just £1.50 (one-off).

Easy-to-use and with an attractive, sturdy design, the stripper is eminently suitable for all types of applications. Among its impressive features are a convenient finger-tip cam adjustment for common wire/cable sizes, comfortable cushion-grip handles, effective return spring and handle lock.

ECW gives a volume discount for orders of 30 or more. **Contact: Electronic & Computer Workshop Ltd Unit 1, Cromwell Centre Stepfield, Witham Essex CM8 3TH Tel: (0376) 517413**

WHAT'S NEW
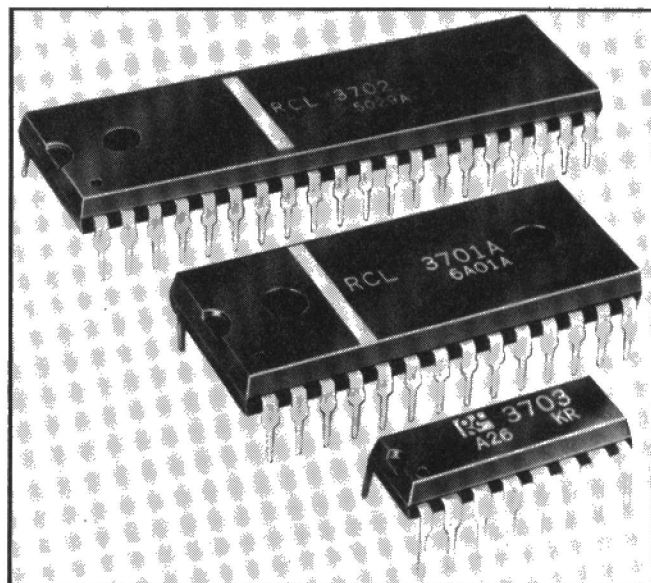
Toko Triad

THREE CMOS LSI integrated circuits, designed specifically for use in numerical control applications, are now available from Cirkit in economical plastic packages. Previous versions of the chips were available in ceramic packages only.

These new Toko ICs, the KM3701AD function generator LSI and the KM3702D comparator LSI, are ideally suited for a variety of factory automation and industrial control applications. They can be used to control robotic systems, milling and drilling machine tools, step and repeat handlers, automatic loaders, process control and other types of product equipment. The KM3703D is a feed-back pulse generator for use with the KM3702D.

The KM3701AD generates interpolation pulses for two axes of movement, according to instructions from a host CPU. It provides a smooth range of motion for a tooling head or robotics device by generating separate interpolation pulses with each feed pulse. In addition, the $\sqrt{2}$ control maintains constant tooling head speed. The KM3701AD provides the flexibility to control linear, circular, parabolic, logarithmic and exponential interpolations.

The clock rate of the KM3701AD is 5Mhz (max.); the interpolation pulse distribution rate is 454.5 KPPS (linear interpolation at 5Mhz clock) and 238.1 KPPS (circular interpolation at 5Mhz clock). Internal registers can be read at any time.

With the addition of the KM3702D comparator LSI, the KM3701AD can be used to control DC servo motors. The KM3702D is a positional control CMOS LSI that provides optimum control of servomechanisms. It closes the positioning loop for a servo motor by counting the difference between command pulses and feedback pulses, and then generates a pattern for use by a D/A converter. When the number of input pulses is equal, the KM3702D provides a signal to stop the motor. The chip interfaces with any 8-bit CPU.

The clock rate of the KM3702D is 1.5MHz (max.); the output pattern is 16 bits (max.); and the velocity of the output pattern is 13.3 micro sec. at 1.5MHz clock.

The Toko KM3703D monitors the direction of rotation of servo motors, as sensed by an encoder, and transmits the information to the KM3702D. This feedback signal is either a positive or negative pulse. It also features a feedback pulse multiplier for increased encoder resolution.

Toko products include numerical control boards, miniature RF and IF filters, and semicoder devices.

A special KM chip numerical control prototyping kit for two-axis control is also now available from Cirkit. It includes one KM3701D, two KM3702D ICs and two KM3703D ICs, as well as complete documentation.

Cirkit Distribution Ltd. Park Lane Broxbourne Herts. EN10 7NQ. Tel: (0992) 444111

Cute Qwerty Mini-Vac

AS a computer accessory, this little tool really has to be my pick of the month.

About twice a year I laboriously strip apart my computer keyboard and clean it out. It is kept in the workshop surrounded by all the paraphenalia of an addicted electronics designer. Inevitably, it picks up the grit and grime that is somehow attracted to any well frequented den. Just as inevitably, the dust creeps in between the keys and the contacts beneath, eventually resulting in loss of typing accuracy as keys misconnect.

All that could now be a thing of the past, thanks to a splendid little vacuum cleaner made by Microphax. It is a well made, compact and portable microcleaner called Mini-Vac.

Unlike compressed air cleaners, which simply disperse the dust particles, Mini-Vac simply vacuums them safely away. It is supplied with a dust filtration bag and a range of interchangeable brushes and extension tubes for reaching into those awkward to get at corners. The basic model is supplied for use with a small nine volt battery,

a PP3 for example. This simply slots into the main handle canister. It will run just as happily from a normal mains operated 9V battery eliminator, such as those used with cassette recorders.

Using Mini-Vac is simplicity itself. Just choose the attachment you want, push the button, and cleanliness re-appears. The bag has cleverly been give a velcro fixing at the rear so that it can readily be emptied.

Fitting neatly into the palm of the hand, Mini-Vac is also ideal for cleaning photographic, video and audio equipment, and costs just £12.95 plus VAT. Microphax can also supply the optional mains adapter at a realistic price.

Even the inside of my computer is now clean – something that I have never risked before for fear that dust particles might contain metallic fragments. If trapped between chip pins, these could cause more problems than any program bug. My clean machine certainly shows that Mini-Vac can reach parts other handi-cans can't.

For further information contact: Microfax Ltd, 36 Nuffield Way, Abingdon, Oxon, OX4 1TF. Tel: 0235 25695.
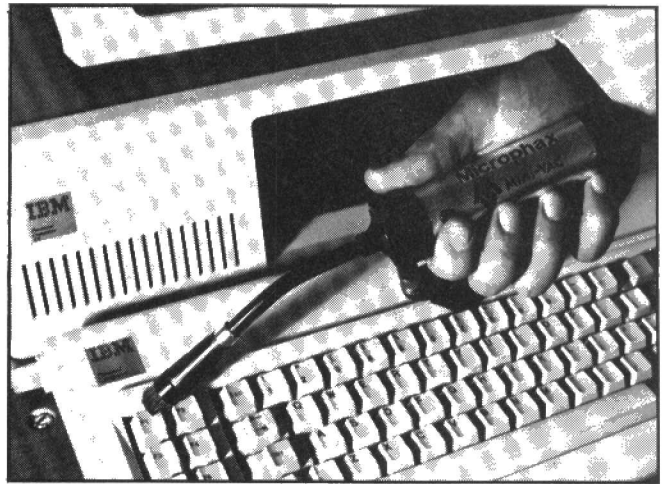
COUNTDOWN

If you are organising any electronic, computing, electrical, scientific or radio event, big or small, drop us a line. We shall be glad to include it here.

PLEASE NOTE: Some events listed here may be trade only, or restricted to certain categories of visitor. Also, please check dates, times and other relevant details with the organisers before setting out as we cannot guarantee information accuracy.

Autumn Course on The Art of Hi Fi. For 10 weeks from Sept 28th 1987. Charles Keene College of Further Education, Leicester. 0533 516037.

Sep 15. Outdoor Sound Propagation (IOA). Open University, Milton Keynes. 031-225-2143.

Sep 15-18. Design Engineering Show. National Exhibition Centre, Birmingham. 01-891-5051.

Sep 15-18. International Conference on Japanese Information in Science Technology and Commerce. University of Warwick. 01-323-7924.

Sep 21-24. Electronic Security and Surveillance 1987 conference. Warwick University. 01-403 2351.

Sep 23-27. Personal Computer World Show. Olympia. 0203 470075.

Oct 6-8. Internepcon Packaging Show. Metropole Convention Centre, Brighton. 01-891-5051.

Oct 13-15. British Laboratory Week '87. Grand Hall, Olympia, London. 0799-26699.

Oct 20-22. International Test & Transducer Exhibition. Wembley Conference Centre. 0822-4671.

Oct 20-22. Testmex. Business Design Centre, Islington, 0799-26699.

Nov 3-5. Custom Electronics and Design Techniques Show. Heathrow Penta. 0799-26699.

Nov 3-Dec 10. Research and Development Society Silver Jubilee Exhibition. The Design Centre, London. 01-235-6111.

Nov 5-8. Reproduced Sound Conference – IOA. Windermere Hydro Hotel. 031-225-2143.

Nov 19-20. Desktop Publishing. Cumberland Hotel, London. 01-871 2546.

Mega Fluke

FLUKE'S position as the world's largest multimeter manufacturer is confirmed with the announcement that the one millionth 70 series model has just come off the production line at the company's Seattle manufacturing facility. To mark the importance of the occasion, the millionth model was gold plated and presented to Chairman John Fluke Jnr. who will place it in Fluke's own museum in Seattle.

The one million 70 Series multimeters are valued at over $130,000,000 (130 million dollars) and Fluke say that they have helped them consolidate their position as the world market leader for these basic tools, which are to the service engineer what a handsaw is to a carpenter. Today Fluke claims about 40% of the world's handheld multimeter business, largely due to the runaway success and innovation of the 70 Series, now in very high volume automated production in Seattle. In addition to the 70 Series, Fluke manufacturers a number of other lines of handheld, benchtop and high-precision multimeters, with worldwide annual sales exceeding $100 million for all. Other product lines built and marketed by the test, measurement and control maker include data acquistion equipment, electronic calibration instruments and systems, and digital testing and troubleshooting equipment. The Company's products are used primarily by commercial electronic manufacturers, military and government agencies, prime and sub-contractors, and utilities in a variety of applications such as research and development, manufacturing, calibration, and service and plant maintenance.

Contact: Fluke (GB) Ltd., Colonial Way, Watford, Herts, WD2 4TT. Tel: 0923 40511.

Widely Spoken

THE first Fane co-axials, the CX12 and CX15 launched at the 1986 Frankfurt Fair, proved largely successful and have been eagerly specified by up-market systems producers such as Stephen Court, and by installation companies as far afield as Thailand, New Zealand and U.S.A. The acclaim with which these handbuilt transducers have been greeted is such that the range has been enlarged by the introduction of 10" and 18" models, the CX10 and CX18, intended for wide range, high quality professional applications; and by three extra high power models intended primarily for stage usage, the CX12PA, CX15PA and CX18PA. The standard CX models feature low reasonance, urethane half roll cone termination and smoothly maintained response up to 20kHz. The P.A. models incorporate a higher reasonance, double half roll suspension and increased magnetic flux to withstand sustained and rigorous stage usage. The 60°x40° integral high frequency constant directivity horn provides wide dispersion coupled with absence of colouration and distortion.

Contact: Fane Acoustics Limited 268 Bradford Road, Batley WF17 5PW, West Yorkshire.

New CB Frequencies

GEOFFREY Pattie, Minister of State for Industry and Information Technology, has announced that a launch date for a new Citizens' Band (CB) radio service on 26/7MHz, will be available from September 1987 and is based on a recommendation by the Conference of European Posts and Telecommunications Administrations (CEPT). It will be available to all CB licence holders under the terms of the existing licence.

CHIP COUNT!

This month's list of new component details received — mainly chips, but other items may be included.

BYV18 series. Schottky-barrier double rectifier diodes (ML).

HB56A19A-B. 9M-bit DRAM module with fast access time and low power (HT).

HM6208. High speed 256K-bit static RAM in 64K x 4 memory configuration (HT).

HM10484-10. One of four new very high speed 16K-bit ECL RAMs (HT).

HM53051P. High performance 1M-bit Frame Memory store (HT).

LM086ALN. 16 character x 2 line dot matrix LCD module with built-in LED backlight (HT).

MAB8032AH. and MAB8052AH. NMOS 8-bit 'state of the art' microcontrollers (ML).

NE-SA5204. High frequency wideband RF and data communications amplifier (ML).

NE-SE5105A. 12 bit high speed precision comparator. Compatible with CMP-05 and RM4805 (ML).

PLH8501-2. Programmable Macro Logic gate arrays in 52-pin PLCC (ML).

SAA1131-1136. Chip set for implementing PCM digital audio on VCRs (ML).

SAA5250. Multistandard teletext CIDAC – CMOS Interface for Data Aquisition and Control (ML).

SMIDs. MELF surface-mounted implosion diode range (ML).

Super-Supply. Claimed to be the smoothest DC output regulator in the world (SG).

Manufacturers and contact telephone numbers for further details. (HT) Hitachi, 0923 46488. (ML) Mullard, 01-580-6633. (SG) Sage Audio, 0274 568647.

Sweltering Superconductors

MITSUBISHI Electric Corporation has successfully developed a ceramic superconductor that carries electric current of 112A/cm2 at liquid nitrogen temperature in a stable condition. The attainment of a current of more than 100A/cm2 represents a great step toward commercialization.

The newly-developed superconductor is barium-yttrium-copper oxide made by an original synthesis and molding method and has superconduction transition starting temperature of 104K and perfect superconduction transition temperature of 95K, the world's top level critical temperature.

In an experiment they succeeded in floating a disk made of this superconductor in room-temperature air by the Meissner Effect, cooling it with liquid nitrogen. In the past, liquid helium was used in such experiments, thus they have attained the world's first success using a superconductor under these conditions.

Gas Pocket

A POWERFUL soldering iron that can be carried in a top pocket, Portasol is completely portable, no larger than a felt-tip pen and offers a range of outputs from 10 to 60W. It is refilled from cigarette lighter butane gas containers, and is suitable for all types of precision soldering, with a choice of tip diameters – 1.0mm, 2.4mm, 3.2mm or 4.8mm. Maximum tip temperatures is 400°C. Safe and reliable, it runs for approximately one hour on a single refill. The clip-on cover has a built-in igniter and, when in position, allows the Portasol to be carried like a pen in a top-pocket.

A powerful gas-operated heater gives a stable output that is superior to battery-operated portable types. This frees the user from having to work near a mains power point or bother with extension cables.

Contact: Freetrade (TEP) Ltd, Moor Lane, Witton, Birmingham B6 7HH. Tel: 021 356 2582.
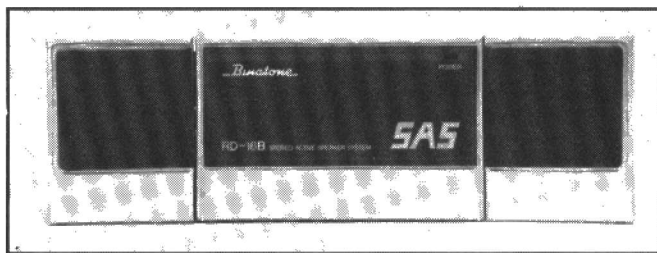
Mini Music Mobilised

BINATONE International Limited, the UK's largest privately owned consumer electronics company, has launched SOUNDPAC – a mini amplified speaker system designed for use with personal stereos.

SOUNDPAC, with its stylish silver finish, is similar in size to a traditional audio cassette box and boasts the following features: built in stereo amplifier; full range dynamic speakers; power on/off LED indicator; extension connection cord; compatibility with personal stereos, portable radios and TVs etc; operation on 2 x R6 batteries.

Gulu Lalvani, Chairman of Binatone International Limited, commented that they are very excited about this innovation since it satisfies a real consumer need for people who have personal stereos, increasing the versatility and value of the product by enabling the consumer to enjoy music anywhere, without the need for headphones. SOUNDPAC typifies the Binatone policy of giving the consumer real benefits at affordable prices and they are certain that this will be proven by the success of this unique product, which became available during May, priced at around £12.99.

Contact: Sue Morris, Morris Media, 26-40 Kensington High St, London W8. Tel: 01-938 2222

Link Trainer

THE Flight Electronics 68000 training system can now be used either in stand-alone configuration, using a terminal as the control console, or in conjunction with a mini or mainframe as a target board.

When attached to a mini or mainframe computer the FLT-68k can be used as a target for 68000 object code. The code may be generated by any cross-assembler or compiler capable of downloading Motorola 'S' format files. A 'transparent mode' in the firmware allows a direct terminal to mainframe link for program generation. The download command then enables the object code to be loaded into the FLT-68k. The training system's debugging facilities may be used to run, test, or modify the program.

Contact: Flight Electronics Limited, Ascupart Street, Southampton SO1 1LU.

Sage Qualities

Sage Audio have introduced two totally new highly advanced audio power amplifiers: the '*superamp*' a **bipolar** amplifier so technologically advanced it out-performs even the very best MOSFET amplifier modules, and the '*supermos*' a **MOSFET** amplifier which includes all the hi-tec features of the superamp but with a MOSFET output stage giving unprecedented speed and performance unmatched anywhere.

The truly monolithic integrated construction includes a high efficiency heatsink, five simple connections, I/P, O/P, +VE, −VE and OV with no external components necessary.

The Sage Audio *Superamp* and *Supermos* modules are based around a completely new design incorporating all the most up to date technical features available anywhere in one (patent pending) unique amplifier.

For fuller details contact: Sage Audio, Construction House, Whitley Street, Bingley, West Yorks, B16 4JH. Tel: 0274 568647.
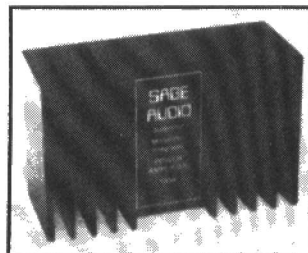
Young Scientists Truimph

Three young British scientists won major recognition in the 19th European Philips Competition for Young Scientists and Inventors held in Paris on 11 June 1987.

From a total of 27 entrants from 14 nations, Peter Badger aged 19 from West Bridgeford School, Nottingham, won an award of 14,000 FF (£1424) for his computerised device for improving table tennis skills. Placed third overall, Peter's invention was praised by the highly qualified scientific judges drawn from 7 countries for its thoroughness in design and its commercial potential.

Youngest contestants of the competition, Andrew Sutton and Nicholas Porter both aged 14, of Aylestone School, Hereford, won Certificates of Distinction, worth 4,000 FF (£407) for their practical device to measure accurately extremely slow speeds of wire drawing in an annealing process, for Messrs Wiggins Alloys of Hereford.

All British winners demonstrated a determination to put technology to work, and showed a mature grasp of practical application of their inventions.

Such tenacity of purpose and eye for the practical does much to dispel criticism that the British have good ideas but do not put them to practical use.

These three contestants were Philips UK finalists in the British Association Science and Technology Awards.

For further information contact: Mr D.C. Whitter, UK Corporate Relations, Philips Electronics, Tel: 01 689 2166 ext 8229, or Mr A West, The British Association of Young Scientists, Tel: 01 734 6010.

London Calling

The London Electronics College will be launching a new series of up-dated one year full-time BTEC National Certificate courses from 21st September 1987.

The subject specialisms available will be: Electronic Equipment Servicing (TV, VCR and CCTV), Computing Technology (Microprocessors, Interfacing and Data Comms), Information Technology (Telecomms, Networks, Satellite TV and CD), Software Engineering (Assembler, BASIC, Pascal, Programming & CADCAM).

These courses are particularly important for those wishing to update or re-train, either with Employer sponsorship (up to £1,000 ATS grant aid) or for those recently taking redundancy.

The College is also a Managing Agency for the MSC Job Training Scheme (JTS) and will recruit suitable applicants direct onto the new JTS. This programme involves periods of job training and work experience in industry; employers interested in taking trainees for 3 to 6 months should also contact the College. (Trainees will receive a full training allowance from the MSC)

Other courses available include a two year full-time BTEC National Diploma and a one year full-time BTEC Higher National (Computing Technology, Control and Robotics). Short courses from 1 to 3 weeks (VCR Servicing and Microcomputer Servicing) are also running. The EITB Certificate of Basic Technician training (Electronic Engineering Applications and Engineering Software Applications) may also be awarded.

For details and prospectus please contact: M.D. Spalding B.Sc. M.Sc. PGCert.Ed. C.Eng. MIEE, Principal, The London Electronics College, Penywern Road, London SW5 9SU.

Girl Technician

The search is now on to find the 1987 Girl Technician Engineer of the Year, nominations for which are required by 5 October.

Sponsored by The Caroline Haslett Memorial Trust and The Institution of Electronics Incorporated Engineers, The Girl Technician Engineer of the Year competition is now in its tenth year.

The aim of this Award – in the realisation that the engineering industry needs to attract more young people of the right calibre – is to focus attention on electical and electronic engineering as a worthwhile professional career for women. By selecting the most outstanding girl Technician Engineer – who will have successfully completed the necessary education and training, and have proved herself capable of holding a responsible job – it is hoped that she will, by her example, encourage more young girls to enter the electrical and electronic engineering profession.

Past winners – all of whom were in their twenties – have ranged from a Development Project Leader to a Contracts Engineer and Assistant Test Manager; and came from the telecommunications, electrical consumer goods, electrical contracting, electricity supply, instrument, food processing and aerospace industries.

Nominations for the 1987 Award with its £250 prize, and for the Caroline Haslett Memorial Trust's Mary George Memorial Prize (£100) – to be awarded to the most promising younger entrant – must be received by no later than 5th October 1987.

Copies of the Award nomination form and brochure are obtainable from: The Secretary, IEEIE, Savoy Hill House, Savoy Hill, London WC2R 0BS. Tel: 01-836 3357

Godiva Boards

The Education Division of Cirkit has acquired exclusive rights to distribute the Godiva range of modular printed circuit boards for use in Primary and Secondary schools by pupils in CDT, Science, Maths and Computer Studies.

The boards have been designed, developed and tested by Coventry Education Authority Microelectronics Centre over a period of four years, during which time they have been used extensively within the Coventry TVEI programme.

The principle of Godiva boards is to promote a systems approach to electronics, encouraging students to analyse, investigate and develop solutions to electronic control problems. Each module performs a single electronic function and although some are more complex than others, each has a specific purpose corresponding to one of the basic circuit blocks used in electronic systems today. Through understanding each function a novice can construct complex electronic systems without the need to understand the circuit theory in detail.

The approach brings the exciting realms of electronics within the grasp of all pupils, obviating the need to study individual components and their characteristics, which has in the past often been a stumbling block for electronic teaching. Furthermore, it is more in line with the requirements of most examination syllabuses in which electronics plays a part.

Godiva electronic modules introduce the subject through the simple classifications of input, process or output, whilst making clear the distinction between hard-wired electronic systems and computer processing software.

Godiva Boards can be interwired to create a great variety of electronic systems, and actual control systems for students' working electro-mechanical projects. Each module adheres to a predetermined electrical specification and is fully interchangeable with others in the range. Quality, long-term reliability and 'survivability' are key features of the products.

LED indicators on all signal outputs provide a visual indication of the circuit in operation, and the physical layout allows digital outputs from two or more boards to be read as a single 8-bit byte.

The boards can be laid out virtually in block diagram form using 2mm plug and lead sets to connect them, but once a working hookup is constructed they can be stacked to form a compact assembly. When stacked, the power supply rails are carried by the metal spacers between the boards, a technique which reduces the 'spaghetti factor' and thus the possibility of confusing power supply lines and signal inputs.

Other modules to be introduced in the future will be an analogue-to-digital converter, EPROM programmer, stepper motor driver and dual liquid crystal display.

For further information contact: Cirkit Distribution Ltd. Park Lane, Broxbourne, Herts. EN10 7NQ Tel: 0992 444111.

THE LEADING EDGE

A dreadful waste all round

Too often people in positions of power squander money and resources in ill-considered and under-informed decisions.
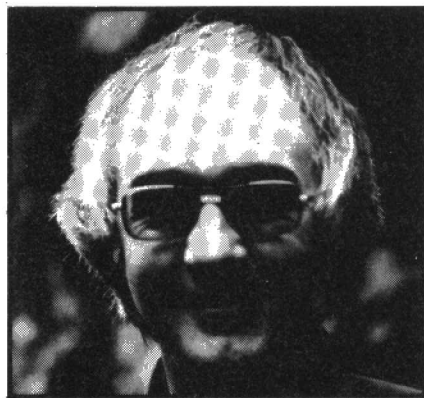
BY BARRY FOX

POLITICIANS, captains of industry and union officials all have one thing in common — they are too busy with too many widely differing projects to be able to dig deep into any one of them. So they must rely on briefing sessions and documents provided by support staff.

Sometimes they get good briefings and read them carefully. Sometimes not. The difference shows.

Middle managers should not need briefings, because their job entails being closer to the grass roots. Sometimes the gap shows.

Two incidents, one on either side of the political fence, highlight the perils of poor briefing.

British Telecom recently announced its Video Map and Imaging System. VMIS is an interactive video system which displays Ordnance Survey maps on a video screen, along with computer graphics and data. BT says the system is ideal for industry, local authorities and emergency services — and costs only a third the price of competitive systems.

VMIS was developed at BT's research laboratories. The control computer is a modified BT M6000 micro, which uses a 32 bit Motorola processor. Up to 55,000 maps are stored on each side of an optical videodisc, with indexing by postal address and grid reference. The computer uses these references to retrieve any map within a few seconds. Graphics can be stored on Winchesters to overlay the map pictures on screen, for instance to highlight the location of fire and police stations.

The demonstration given of how VMIS can be used to guide ambulance crews to the scene of an accident was less than impressive. Instead of just sending out a radio call with the name of the street, and letting the crew use their taxi-type knowledge of the area, the computer operator entered map references, patient names and moved cursors across the screen before calling out.

"Poor chap would be dead by now" said one journalist who was watching.

Although doubtless VMIS will be a boon to some, the quoted prices are likely to hang like a millstone round BT's neck. BT talks of a 2 gigabyte disc store for the graphics, but the quoted system price of £30,000 includes only a 170 megabyte disc.

In answer to questions for which the BT managers were all too clearly ill prepared, the price of the videodiscs was put at £250 each, with the map content tailored to an individual user's needs. IV engineers confirm that this is an absurdly uneconomical way of producing video-discs. The paper maps must be photographed with a rostrum video camera and the images recorded on video tape from which the Philips disc factory at Blackburn makes a master disc. Saleable discs are then replicated by pressing from this master.

BT promises a turn round time of 4–6 weeks for tailored discs. Photographing maps is a tedious business and the Philips disc factory in Blackburn charges up to £3500 to make the master disc; each single-sided disc pressed from the master then costs up to £60. Prices only fall if many hundreds of discs are pressed and the factory is given several weeks to turn round the order. But BT has promised a total turnround of 4–6 weeks. Now, after collecting their thoughts, the BT people say that only some discs will be "bespoke". Others will be standard discs with the whole of the UK mapped. These will cost £250.

But the price does not include the copyright fees payable to the government Ordnance Survey. At the VMIS unveiling BT said it did not know how much OS would charge. But the next day OS told me that BT's customer will have to pay a royalty of £2.25 per map per year. Large scale coverage of the London area would need 6500 maps. So each disc would attract an annual licence fee of £14625.

Now BT says that OS will charge a one-off fee of £510 for the standard disc and there would be no royalty even on bespoke discs. It all gets very confusing.

The real surprise is that the division of BT selling VMIS was unaware that another division of BT was about to announce the purchase of another quite different, and incompatible, IV system for staff training. This is based on the Videologic system which links any IBM PC clone to any professional videodisc player, running any type of optical video disc. Because of this flexibility the Videologic system has become a de facto standard in the IV industry.

Because the VMIS people at BT hadn't heard about Videologic they also didn't know that there already exists a map video disc which can be bought for use with the Videologic system. It's made by a firm called Action Information Management in Wiltshire. The AIM disc covers the whole of the UK and, with retrieval software and Ordnance Survey royalty, costs £7,200. Car rental firms already use the disc and Videologic interactive video system to help engineers find breakdowns.

A few days after the VMIS launch, two unions called a press conference that, on its own way, was equally poorly prepared.

It followed the decision by British Satellite Broadcasting, BSB, to buy its direct broadcasting satellites from the Hughes Aircraft Company instead of British Aerospace. Manufacturing union TASS and the technicians' union ACTT, were trying to save members' jobs by objecting to the foreign deal.

But the unions' case was seriously undermined by wild accusations which they could not back up, and which showed surprising naivety over the technical problems facing the satellite industry.

General Secretaries Ken Gill of TASS and Alan Sapper of the ACTT claim that the deal struck between Hughes and with BSB, will give Hughes and its parent General Motors control over BSB's affairs and the programmes broadcast. But neither union has any evidence to offer in support. BSB denies that Hughes will get any equity or say in running of the company. "It is loan financing only" says BSB.

British Aerospace has already lost one chance to supply satellite hardware. In March 1982 the Home Office gave the BBC a licence to start DBS in 1987, but said that the satellite must be bought

Advertisements
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AN EXCLUSIVE TECHNOLOGY?

*E*LECTRONICS *is a technology that has always been well suited for amateur participation. Since the introduction of the thermionic valve, and no doubt before that, home based experimentation has produced numerous inventive ideas. Aided by the various electronics magazines, the tradition has continued on through the introduction of transistors, integrated circuits, punched laminate and printed circuit boards. Although each generation of new devices has brought more sophistication, in general, the bulk of electronic technology has been available to amateurs, despite a time when some manufacturers denied hobbyists access to some areas of active devices. Fortunately that attitude died, and the value of hobbyist involvement was recognised for both its sales potential and its creative worth.*

However, an interesting situation is now developing with regard to a rapidly emerging technology, that of Surfce Mounted components. The advantages of SM technology are particularly significant for large commercial manufacturers, since the components are without legs or wires, and are soldered directly to the conductive tracking on printed circuit boards. Practically all groups of components are now being manufactured for surface mounting. Their nature drastically cuts down, and in many cases eliminates, the need for holes to be drilled or punched in PCBs. Obviously this reduces some processing costs, but in particular it also results in a marked decrease in component size. Consequently component packing density per board increases, and track lengths are shortened, so speeding signal transfer times.

The interesting question though, is whether or not amateur inventiveness will be up to finding ways in which to use this new technology. The problem appears to be that of soldering the components without the use of sophisticated automatic equipment. Presently, this sort of equipment is highly expensive, and for the immediate future will probably remain outside the reach of any but the largest organisations.

Although there is no doubt that components in standard legged packages will remain with us, there are already some components that are only manufactured for SM use. Whilst special sockets are made for some SM devices to be mounted on conventional PCBs, the SM-only trend will continue.

One side effect for amateur constructors is that the prices of conventional parts may increase as more emphasis is placed on SM quantities by the main consumers, leaving only a relatively small market for some normal types.

Amateurs have little control over this latter aspect, but regarding the use of SM parts, PE and other magazines may perhaps eventually be publishing SM-orientated constructional articles, though currently it seems impractical. However, the amateur electronics enthusisast is frequently full of bright ideas, so I look forward to seeing how inventiveness might cope with this apparently sophisticated assembly problem.

THE EDITOR

PLEASE NOTE OUR NEW ADDRESS

Much cheaper than a proprietary system, and an ideal way to use up those unwanted analogue synths, this interface uses a +5V gate signal to trigger a synth over at least three and a half octaves.
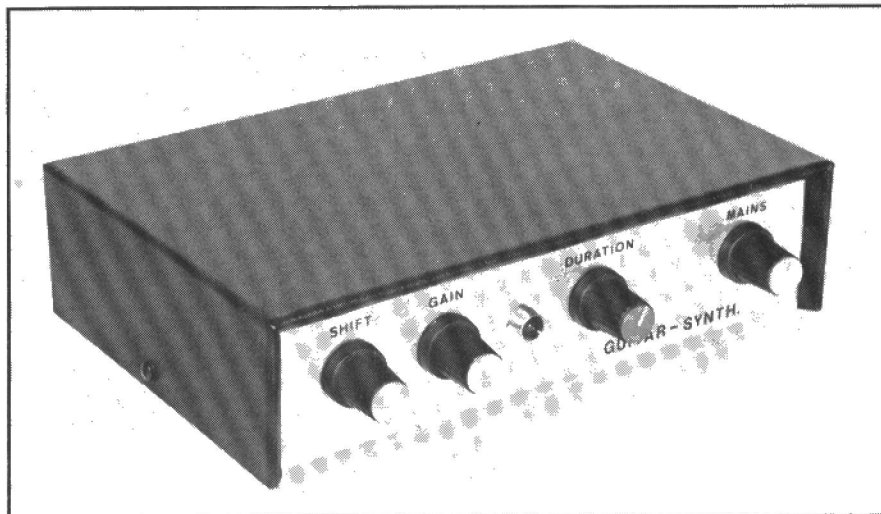
GUITAR TO SYNTH INTERFACE

BY ROBERT PENFOLD

Turn your axe to ivory

Electric guitars remain very popular, but have perhaps given way slightly to keyboard instruments in recent years. One likely reason for this is the greater versatility of electronic keyboard instruments. Obviously there are a great many effects units that can modify the sound produced by a guitar, but even with a dozen of these the range of sounds would probably not equal that of even one of the cheaper keyboard instruments.

Perhaps the obvious answer to the problem is to have a synthesizer controlled from the guitar in some way, rather than to buy numerous effects units. This is a much neater solution which enables the guitarist to obtain any electronic keyboard sound. Unfortunately, it tends to be a rather expensive way of doing things. Quite good results can be obtained using a simple unit such as 'Guitar Tracker' which was described in the June 1986 issue of PE, but a much wider range of sounds can be obtained by interfacing the guitar to a full analogue synthesizer. This is becoming an attractive method as analogue synthesizers now seem to be widely regarded as out-of-date. Many guitarists will have access to an otherwise unused instrument, or secondhand (pre-used?) instruments can be obtained at surprisingly low cost.

This only leaves the problem of a suitable guitar to synthesizer interface, which is the purpose of this project. The device covers several octaves, should handle any note that an ordinary (non-bass) guitar can produce, and provides a standard 1 volt per octave logarithmic output. A gate signal is needed to drive the "gate in" or "trigger in" input of the synthesizer, and two gate outputs are provided. One of these simply provides a gate pulse while the input signal is above a certain threshold level. The other gives an output pulse which has a preset duration of between about 35ms and 750ms. The second gate output is very useful as many synthesizer sounds are dependent on a short gate pulse duration, and a very brief gate signal cannot be obtained reliably from the other gate output.

SYSTEM OPERATION

The block diagram of Fig.1 shows the general set up used in this interface. The top row of blocks are concerned with the generation of the output control voltage, while the lower row of blocks are primarily needed to generate the gate pulses (although these stages do play some part in reliably generating the right output voltage).

Starting with the top row of blocks, the input signal is first fed to an amplifier where it is boosted to a high enough
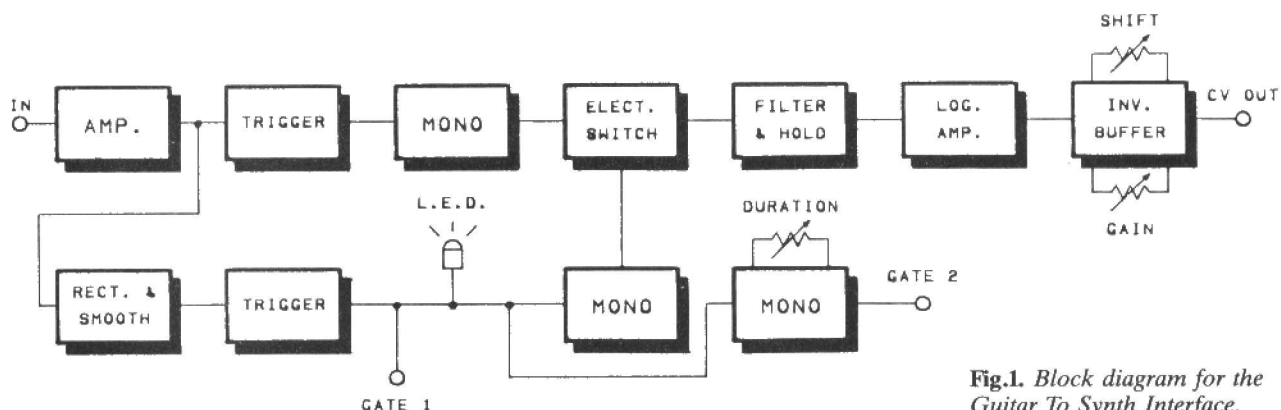

Fig.1. *Block diagram for the Guitar To Synth Interface.*

level to drive the next stage properly. This is a trigger circuit which has a large amount of hysteresis. The latter is essential due to the unusual and ever changing waveform produced during the course of each guitar note. The hysteresis ensures that the output from the trigger circuit is a pulse waveform at the same frequency as the fundamental input frequency.

The next stages form a simple frequency to voltage converter, and the monostable multivibrator forms the basis of this section of the unit. The monostable is a retriggerable type, but it is preceded by a simple pulse shaper circuit which always provides brief trigger pulses, regardless of the mark-space ratio of the output signal from the trigger circuit. The output pulse duration of the monstable can therefore be regarded as fixed and independent of the input signal. The pulse frequency is equal to the frequency of the input signal.

from the monostable to give a d.c. output having a reasonably low ripple level. This part of the unit differs somewhat from the equivalent circuit in the 'Guitar Tracker' project, where a simple single stage passive filter was used, followed by a high input impedance buffer amplifier. The latter gives a 'hold' action, so that the output voltage is maintained when the electronic switch is opened and the signal from the monstable is cut off.

In this article a third offer (18dB per octave) active filter is used, but this is based on a buffer amplifier which has an extremely high input impedance so that it still gives a 'hold' action when the signal from the monostable is cut off. The advantage of the active filtering is that it enables the unit to respond rapidly to changes in the input frequency, but with a very low ripple level on the output voltage still being obtained. This ripple is not of great importance in itself, as it tends to have no noticeable effect on the

(i.e. the voltage doubles for each octave increase of the input frequency). Some older synthesizers have control voltage inputs that are compatible with a linear input signal, but most instruments require a 1 volt per octave (logarithmic) control voltage. The output from the filter and hold circuit is therefore fed to a logarithmic amplifer which makes the necessary voltage conversion. In fact the output from this circuit requires some further processing, as it inverts the signal, and does not give a properly scaled output anyway. An inverting amplifier having gain and voltage shift controls is therefore used to process the output from the logarithmic amplifier and give a signal that drives the control voltage input of the synthesizer properly.

The 'gate 1' output signal is generated by rectifying and smoothing some of the output from the input amplifier. This gives a d.c. output signal which is roughly proportional to the audio input
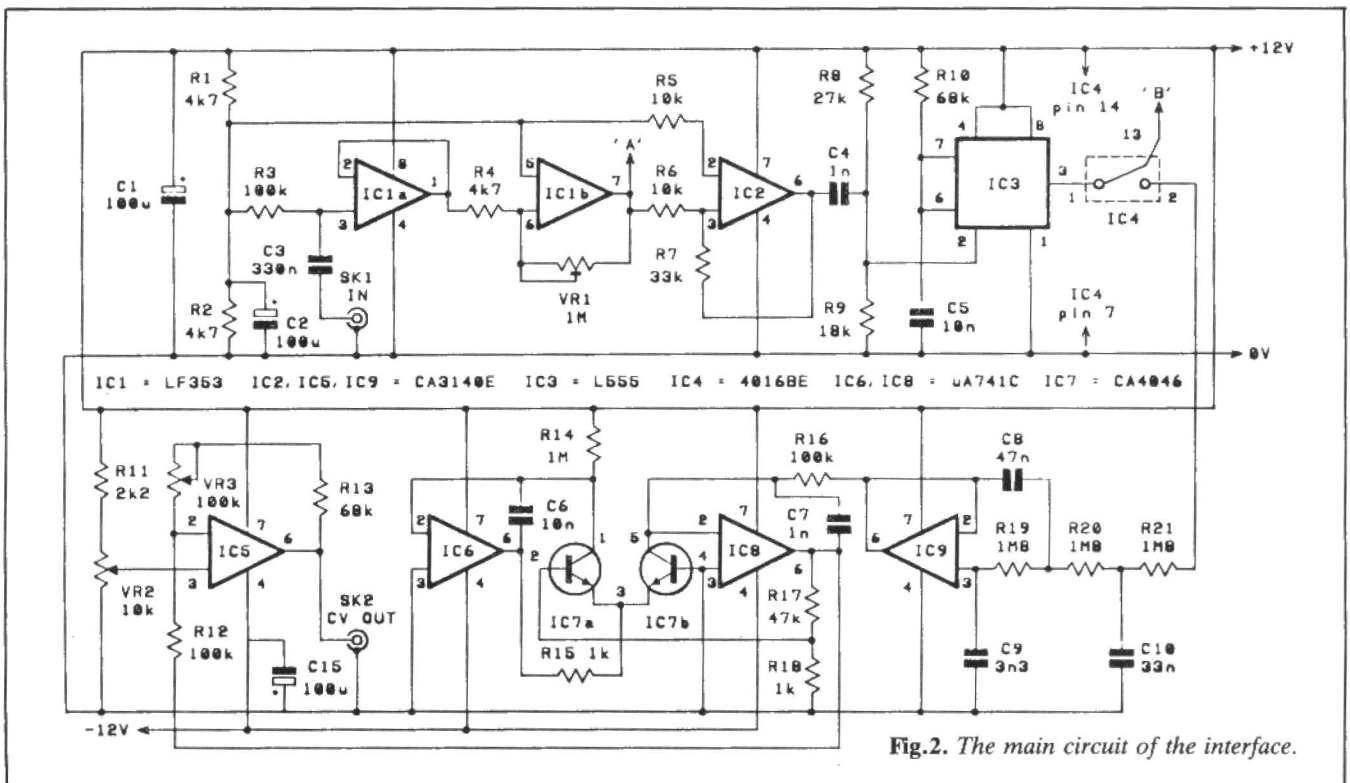

Fig.2. The main circuit of the interface.

Therefore, as the input frequency increases, the monostable's output pulses become bunched closer and closer together, and the average output voltage increases. In fact there is a linear relationship between the input frequency and the average output voltage. This section of the unit is actually very much the same as the circuit in the 'Guitar Tracker' project referred to earlier, and this article should be consulted if more concise information on operation of the frequency to voltage converter is required.

If we ignore the electronic switch for the moment, the next stage of the voltage to frequency converter is a lowpass filter. This simply smooths out the pulses

output from the synthesizer. It can indirectly produce a noticeable effect though, when the signal from the mono-stable is disconnected by the electronic switch. The output voltage is then maintained at whatever level it happened to have at the instant the electronic switch was opened, and any ripple can result in the 'held' output voltage being slightly above or below the correct level. This is reflected in the note from the synthesizer being slightly off-tune. Active filtering enables the unit to respond to changes in the input frequency with suitable rapidity without having to compromise the pitch accuracy on 'held' notes.

The output voltage from the filter and hold circuit has a linear characteristic

level. This signal is fed to a trigger circuit which provides a high gate signal if the input signal is above a certain level. The output level from a guitar can be slightly erratic, and so this trigger circuit is given a certain amount of hysteresis so that problems with multiple gate pulses on each note are avoided. A l.e.d. indicator shows the signal level on the 'gate 1' output, which can be quite helpful, especially when initially setting up.

This gate signal is fed to the inputs of two non-retriggerable monostable multivibrators. One has a fixed output duration and is used to drive the electronic switch, while the other has an adjustable pulse length and provides the 'gate 2' output signal.
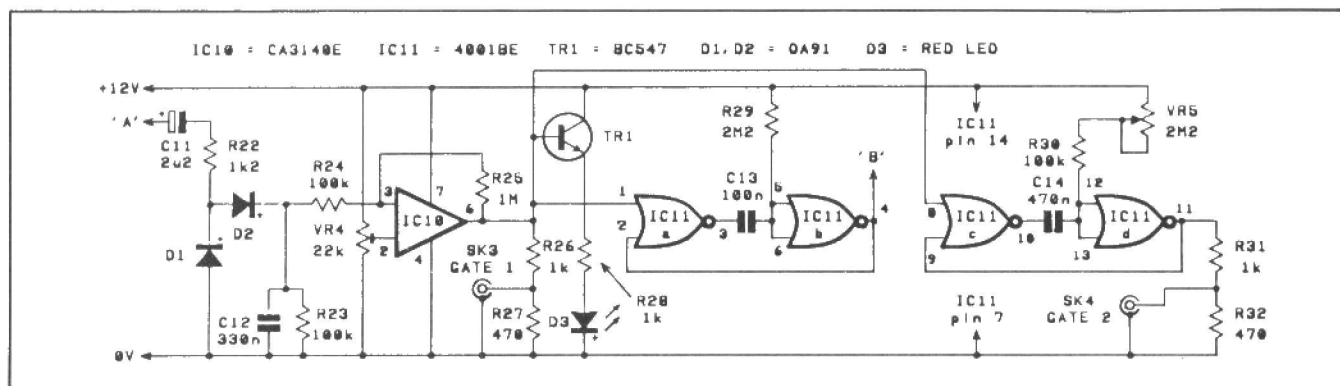
Fig.3. *The gate pulse generator circuit.*

At first sight the electronic switch and the 'hold' circuit might seem to be irrelevant, since the guitar will normally provide a significant output level while it is being played. In practice there are a couple of problems if these circuits are omitted. One is simply that the synthesizer will be capable of producing a wide variety of envelope shapes, including some with quite long release periods. With an envelope shape of this type there is a real danger of the note from the guitar ceasing before that from the synthesizer has fully decayed. With the 'hold' circuit included this does not matter, since the output voltage will be maintained for a reasonable period of time regardless of whether or not the guitar is still providing a significant output level.

The second problem is one of spurious output signals from the guitar while it is being played. Even an accomplished player is unlikely to play each note perfectly, instantly snapping from one note to the next. This does not tend to be noticeable on the direct output from the guitar, as any spurious signals are accepted by the listener as ordinary and acceptable guitar sounds. The result on the output from the synthesizer can be slightly catastrophic though, with the pitch tending to jump all over the place during the transition from one note to the next. This gives an output signal that can be far from musical, and in an extreme case can be more reminiscent of cats in the night than a musical instrument.

The system used here has the electronic switch closed briefly at the beginning of each new note. This gives the filter and hold circuit time to adjust to the new frequency, and it then holds this level until a new note is triggered. Any spurious 'buzzes' or other sounds in the intervening period will not affect the output voltage. This system does not absolutely guarantee a perfect output from the synthesizer, but in practice most problems seem to result from one note being damped prior to the start of the next one. This system eliminates the damping problem and seems to give very reliable results. It can only be defeated by some very inept fingering, or

'machine gun' style playing which is simply beyond the tracking ability of the unit.

CIRCUIT OPERATION

Fig. 2 shows the main circuit diagram for the guitar to synthesizer interface, but the gate pulse generator circuit is shown separately in Fig. 3.

The amplifier, trigger, and monostable stages are virtually identical to those in the 'Guitar Tracker' project, the only difference being that VR1 has been made slightly higher in value so as to boost the maximum available gain. This gives a very wide gain adjustment range, and the circuit can be set up to work reliably with almost any guitar pick-up. There is actually another minor modification to the original circuit in that R10 has been made somewhat lower in value. This increases the maximum input frequency that the unit can handle. This frequency is the one where each output pulse lasts more than one input cycle. This results in the monostable only triggering on every other input cycle, and the average output voltage drops to only half the correct level. With the specified timing component values the circuit will operate properly with input frequencies of up to around 1.35kHz, which should be adequate in practice.

A CMOS analogue switch acts as the electronic switch, and this works well in the present application where an extremely high 'off' resistance is required. The switch is one of the four SPST types in a 4016BE package, and the other three switches are simply ignored.

IC9 acts as the buffer amplifier in the filter and hold circuit, and this is a MOS input device which provides an input resistance of about 1.5 million megohms. This is high enough to ensure that the 'held' output voltage is maintained accurately for at least a few seconds, which should be more than adequate in practice. The filter is really just a standard third order type, but the filter components have been given values that produce a very low cutoff frequency of only about 6Hz. The cutoff frequency has to be a compromise between fast response time and good smoothing of

the d.c. output signal, and 6Hz seems to be about the optimum cutoff frequency. Note that the CA3140E used for IC9 is a type that will operate properly without a negative supply, and that few other types have the correct characteristics for correct operation in this circuit.

The logarithmic amplifier is based on IC6 to IC8. In common with most circuits of this type, it relies on the forward transfer characteristic of a silicon diode to give the right input/output voltage conversion. When forward biased in the manner shown in Fig. 4, a silicon diode (or transistor base-emitter junction) produces an output voltage that is around 0.65 volts. Although circuits of this type are often used as low voltage regulators, the output voltage does in fact increase by about 60 millivolts per decade increase in the bias current. This is normally considered to be a flaw in the efficiency of the voltage regulator circuit, but it provides what is essentially the right kind of conversion for this application. However, in a practical circuit there are two problems to be overcome. One is simply to boost the output voltage to give the required scaling and to remove the offset voltage.
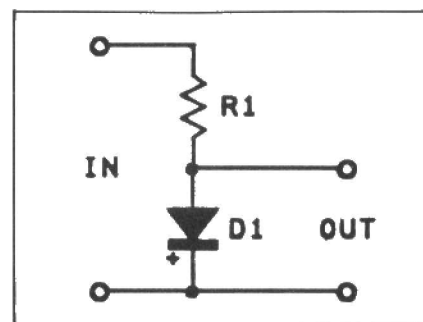

Fig.4. *The basis of a lin./log. converter is just a forward biased silicon diode.*

The other problem is more difficult to combat, and is severe temperature drift that occurs with the basic circuit. Circuits of the type shown in Fig. 4 are often used as temperature sensors, and give a reduction in output voltage of about 2 to 3 millivolts per degree Celsius increase in temperature. The change in output voltage due to temperature drift is not very large, but voltage changes

are considerably amplified in this case, and without some form of temperature compensation this type of circuit is practically unusable. In this case a form of bridge circuit is used, with one section providing the voltage conversion and the other giving temperature compensation. The two transistors are part of the CA3046 integrated circuit which is a five transistor array. Having the two transistors on the same chip gives more effective temperature compensation than using discrete transistors.

IC5 acts as the inverting amplifier, and this has VR2 and VR3 as the shift and gain controls respectively. The general idea is to adjust VR2 for the correct output voltage with a low frequency input, and then to adjust VR3 for the right output potential with a much higher pitched input. By repeating this procedure a few times the unit can be made to track correctly over a wide range of notes. Even with the aid of temperature compensation and using stabilised supply rails, the unit cannot be guaranteed to be drift-free. VR2 and VR3 have consequently been made front panel controls rather than preset types so that the unit can easily be retrimmed from time to time if this should prove to be necessary.

Turning now to Fig. 3 and the gate pulse generators, the amplified signal from IC1 is rectified and smoothed by D1, D2, and C12. The attack time of the smoothing circuit is very short, and although substantially longer, the decay time has also been kept fairly short (about 30ms). For the unit to operate properly it is essential that the voltage across C12 decays significantly during the brief pause between one note and the next, so that the electronic switch is reactivated on each new note. Failure of the unit to trigger on a new note will result in the old note voltage being held, as well as no new gate pulse being generated. IC10 is the trigger circuit, and is a standard operational amplifier type with hysteresis provided by R25. VR4 is the trigger sensitivity control, and this is adjusted to give optimum reliability. D3 is a l.e.d. indicator which is switched on when the output of IC10 is high, and it is driven via emitter follower buffer amplifier TR1. IC10 is powered from a +12 volt supply, but most synthesizers require a +5 volt trigger pulse. R26 and R27 form an attenuator which reduces the output voltage to a suitable level.

The two monostables are both based on CMOS 2 input NOR gates connected in a conventional non-retriggerable configuration. IC11a and IC11b form the monostable which drives the electronic switch, and this circuit has a fixed output pulse duration of around 150ms. This circuit must provide a pulse length that is adequate to let the output voltage adjust to the correct level before the electronic switch is cut off, but it must also be short enough to guarantee that
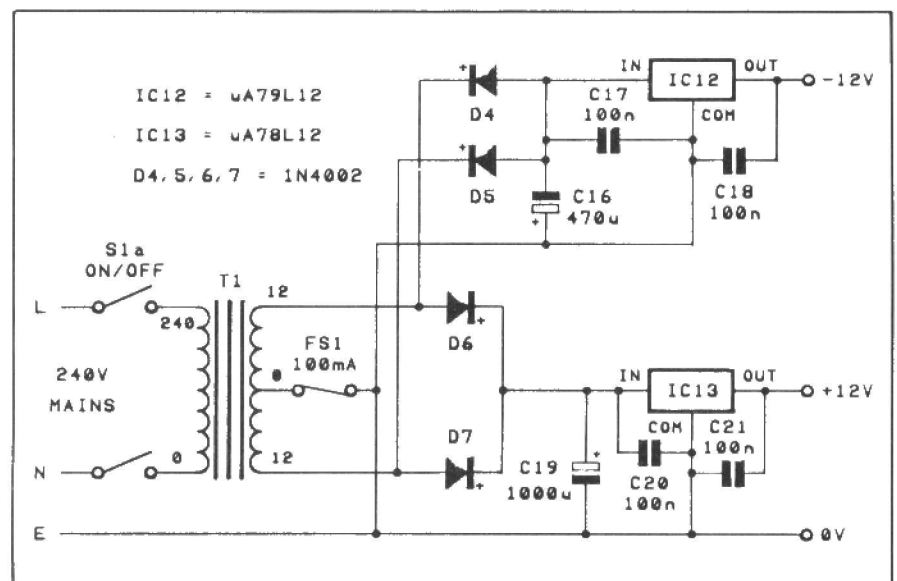
the pulse ceases before another note commences. A time of about 150ms seems about right for my playing, but a different pulse length can be used if necessary. The pulse duration is proportional to the value of R29.

IC11c and IC11d form the monostable that provides the alternative gate pulse signal. VR5 is the gate pulse duration control, while R31 and R32 are an attenuator which provide an output level that is compatible with standard 5 volt logic circuits.

POWER SUPPLY

The unit requires dual balanced 12 volt supplies which must be well smoothed and stabilised. Fig. 5 shows the circuit diagram of the mains power supply unit.

The circuit uses two push-pull style full-wave rectifier and smoothing circuits; one to provide the negative supply and one to give the positive supply. Regulation of the negative and positive supply rails is provided by IC12 and IC13 respectively. These are 100 milliamp types, and these are more than adequate as the current consumption from neither rail approaches anything like this figure.

CONSTRUCTION

Most of the components fit onto the two printed circuit boards. One board accommodates the main circuit (Fig. 6) while the other is for the power supply (Fig. 7). Construction starts with the boards, and the power supply board is very simple indeed. However, the two electrolytic capacitors must be reasonably compact printed circuit mounting types if they are to fit onto the board correctly.

The main printed circuit board is very much more complex, and is less straightforward to build. The first point to keep in mind is that IC2, IC4, IC9, IC10, and IC11 are all MOS input devices, and that the normal anti-static handling precautions should be observed when dealing

with these components. I would recommend the use of sockets for all eleven integrated circuits on the main board — MOS types or not. D1 and D2 are germanium diodes, and these tend to be somewhat less hardy than the more familiar silicon variety. They are slightly more vulnerable to physical damage, but of greater importance, they are much more easily damaged by heat. I have not found it necessary to use a heatshunt when fitting germanium semiconductors, but the soldered joints should be completed with the soldering iron being kept in place for no longer than is really necessary.

Several link wires are needed, and 22 s.w.g. tinned copper wire is suitable for these, or trimmings from resistor lead-outs can be used. If the capacitors are to fit onto the board neatly it is essential that they are of the correct types. The electrolytic capacitors are all radial (single-ended) components, and the polyester capacitors are 7.5 millimetre (0.3 inch) pitch printed circuit mounting components. At this stage only single-sided pins are fitted to the boards at the positions where connections to off-board components will eventually be made.

The case I used is a metal instrument type having approximate outside dimensions of 200 by 130 by 50 millimetres. This represents the smallest size of case that will house all the components without having to resort to an imaginative layout in order to find space for everything. The four sockets are mounted on the rear panel, and standard jack sockets are probably the most convenient type to use. However, you can obviously select any type that fits in well with your other equipment. The panel mounting fuseholder is also mounted on the rear panel, well towards the left hand end of the panel (as viewed from the rear). It is advisable to mount SK1 right at the other end of the panel so that the input

Fig.5. *The circuit diagram for the mains power supply.*

Fig.6. *The Main Printed Circuit Board*
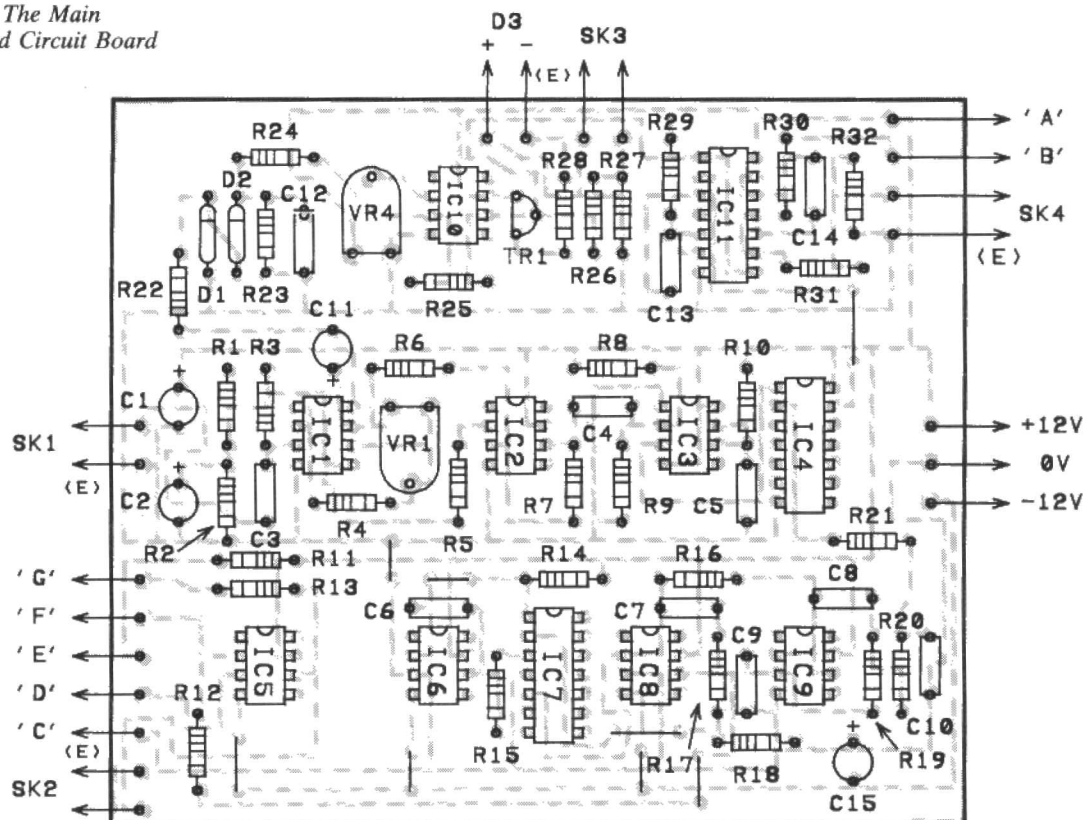
wiring is kept well away from the power supply wiring. An entrance hole for the mains lead is drilled alongside the fuseholder, and this hole should be fitted with a p.v.c. grommet to protect the cable.

The controls and l.e.d. indicator are mounted on the front panel, with S1 well towards the right hand end of the panel and well separated from the other front panel mounted components. The two printed circuit boards are mounted on the base panel with the main board as far over to the left hand side of the unit as possible. This leaves sufficient space for the other board and T1 at the other end of the unit. Either spacers must be used over the mounting bolts for the boards or plastic stand-offs must be used to mount them. A soldertag fitted on one of T1's mounting bolts provides a chassis connection point.

The hard-wiring is fairly simple, but Fig. 8 should help to clarify any minor difficulties. The most likely cause of confusion is mains transformer T1. Most mains transformers these days seem to have twin secondary windings instead of the centre tapped arrangement. However, these can be used as centre tapped types by bridging a '0' and '12' tag (to act as the centre tap), as shown in Fig. 8.

TESTING

With any project it is advisable to have a thorough check over the wiring prior to switching on, but this is even more important with a mains powered project such as the present one. SK1 connects to the guitar by way of a standard jack lead, and initially no connection to the synthesizer is needed. Start with VR1 and VR4 at roughly mid settings. Playing notes on the guitar will probably cause D3 to flash on each time a note is played, but if not, try setting VR1 for a higher resistance (which gives increased gain). The ideal setting for VR1 is one which gives sufficient gain for reliable triggering, but does not give so much gain as to produce unwanted triggering of the unit. Try VR4 at various settings as well, in an attempt to find the optimum settings for these two presets. Setting VR4 for a high level of sensitivity (the wiper well towards the earth end of the track) is unwise as the trigger circuit may have a reluctance to switch off between notes. At the other extreme, the trigger circuit may fail to operate, or it may be rather slow in doing so.

When correct triggering of the unit is obtained, try connecting the control voltage output and one of the gate outputs to the relevant inputs of the synthesizer. Remember that the synthesizer may not automatically switch over to automatic control, and that some manual switching might be needed in order to enable external control. The synthesizer's manual should give details of the correct switch settings where appropriate. Aligning the unit is quite simple, and it is a matter of first hitting a low note on the guitar and adjusting VR2 for the correct note from the synthesizer. Then play a much higher note and adjust VR3 for the correct pitch from the synthesizer. Repeat this procedure a few times until the synthesizer is tracking the guitar properly.

With most analogue synthesizers it is possible to switch the unit up or down by one octave, or even two octaves. A little experimentation might therefore be needed in order to find the right setting to give correct tracking over a
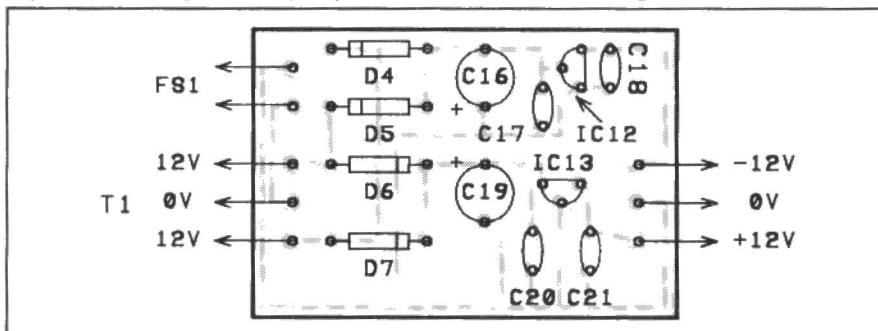
Fig.7. *Details of the power supply board.*

Fig.8.
Unit wiring

THE PRINTED CIRCUIT BOARD IS
AVAILABLE THROUGH THE PE PCB
SERVICE AND A FULL KIT OF PARTS
MAY BE BOUGHT FROM MAGENTA
(ADDRESS IN ADVERT)
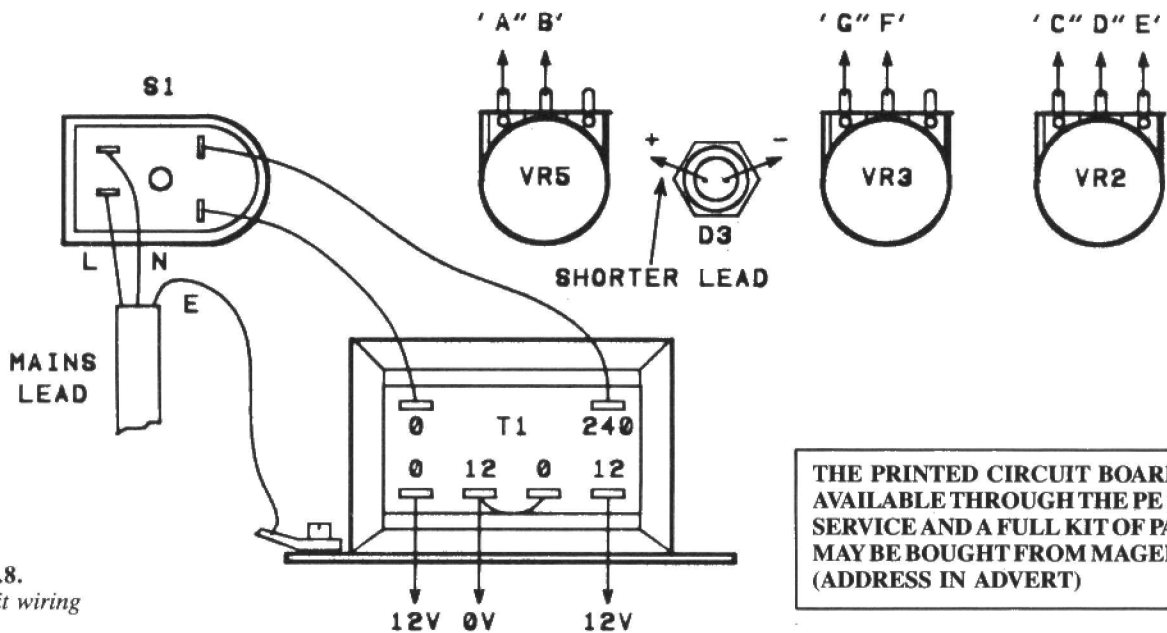
COMPONENTS...

RESISTORS

R1,2,4	4k7 (3 off)
R3,12,16, 23,24,30	100k (6 off)
R5,6	10k (2 off)
R7	33k
R8	27k
R9	18k
R10,13	68k (2 off)
R11	2k2
R14,25	1M (2 off)
R15,18,26, 28,31	1k (5 off)
R17	47k
R19,20,21	1M8 (3 off)
R22	1k2
R27,32	470 (2 off)
R29	2M2

All resistors ¼ watt 5% carbon

POTENTIOMETERS

VR1	1M sub-min hor preset
VR2	10k lin
VR3	100k lin
VR4	22k sub-min hor preset
VR5	2M2 lin

CAPACITORS

C1,2,15	100μ 16V radial elect (3 off)
C3,12	330n poly layer (2 off)
C4,7	1n poly layer (2 off)
C5,6	10n poly layer (2 off)
C8	47n poly layer
C9	3n3 poly layer
C10	33n poly layer
C11	2μ2 63V radial elect
C13	100n poly layer
C14	470n poly layer
C16	470μ 25V radial elect
C17,18,20,21	100n ceramic (4 off)
C19	1000μ 25V radial elect

SEMICONDUCTORS

IC1	LF353
IC2,9,10	CA3140E (3 off)
IC3	L555
IC4	4016BE
IC5,6,8	uA741C (3 off)
IC7	CA3046
IC11	4011BE
IC12	uA79L12 (−12V 0.1A reg)
IC13	uA78L12 (+12V 0.1A reg)
TR1	BC547
D1,3	OA91 (2 off)
D3	Red panel l.e.d.
D4,5,6,7	1N4002 (4 off)

MISCELLANEOUS

SK1,2,3,4	Standard jack socket (4 off)
S1	Rotary mains switch
T1	12−0−12 250mA mains transformer
FS1	100mA 20mm anti-surge

Metal instrument case about 200 × 50
× 130mm, printed circuit boards (2 off),
20mm panel mounting fuseholder, control knob (4 off), 8 pin DIL IC holder
(8 off), 14 pin DIL IC holder (3 off),
fixings, wire, solder, mains lead and
plug.
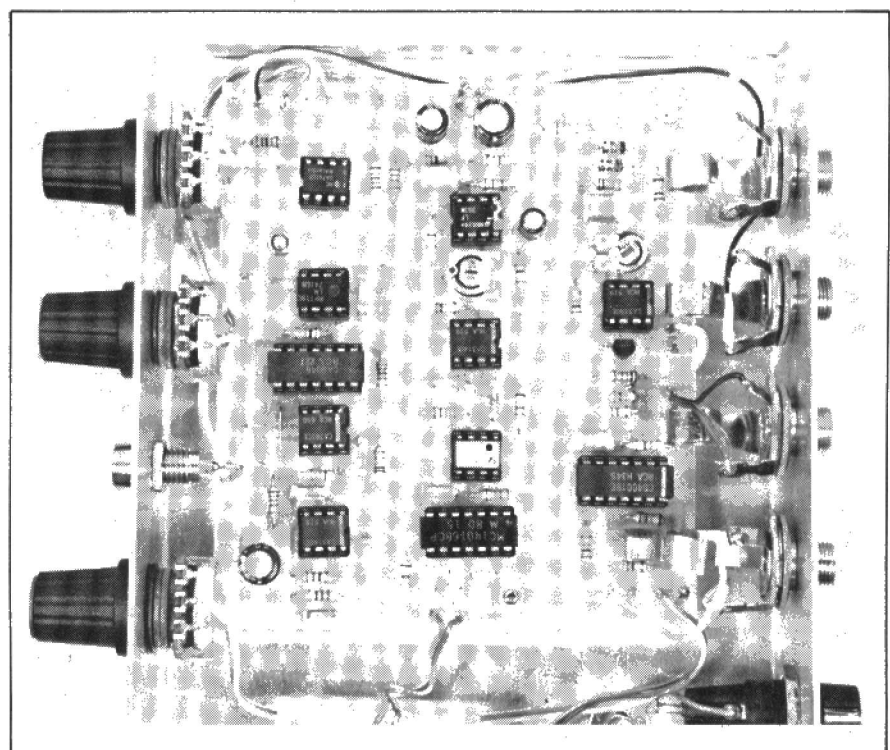
wide frequency range. Of course, it is quite in order to have the synthesizer playing a different octave to the guitar, or with any offset you desire that is within the capabilities of the instrument.

TRIGGER HAPPY

Most synthesizers will trigger properly from the +5 volt gate signals. Some instruments require a +15 volt gate signal, but they are mostly +5 volt compatible as well. If necessary though, a higher output voltage can be obtained by removing R27 and R32, and replacing R26 and R31 with shorting links. Some synthesizers require a 'short-to-ground', gate signal, and these can be triggered by omitting R26, R27, R31, and R32, and using a driver circuit of the type shown in Fig. 9. A few synthesizers require a negative gate signal, and these could only be driven from the unit properly if a suitable voltage shifting circuit was added at each gate output. It should be possible to properly drive a synthesizer having a linear control voltage characteristic if the logarithmic amplifier and inverter are omitted, and the control voltage is taken from pin 6 of IC9. However, in order to obtain usable results it would probably be necessary to add some processing in order to give a suitable output voltage range. **PE**

PHOTOGRAPHS OF THE GUITAR TO SYNTH INTERFACE: ABOVE, THE REAR OF THE UNIT. BELOW, THE FRONT PANEL
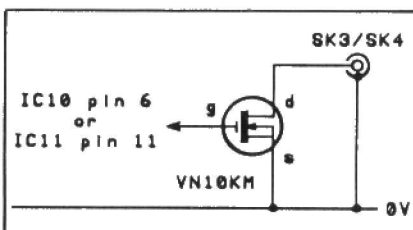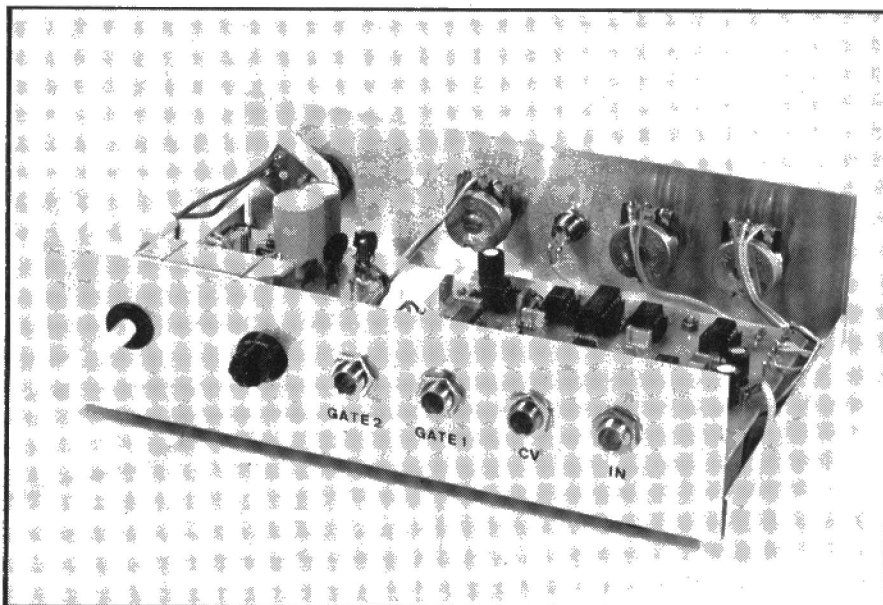
Fig.9. *A short-to-ground output stage.*

PROGRAMMABLE LOGIC DEVICES

PART ONE BY CHRIS KELLY

The logic of digital circuits surely implies that logic devices should help to form them. This is becoming a reality as the PROM principle is extended to simulate new circuit designs.

When is a PROM not a PROM? When it's a PLD

IMAGINE that you are a designer of digital circuits. Your design concept is on paper and you wish to see it as a working system as soon as possible. You reach for a small IC from a storage cabinet and place it in a socket on a device which looks like a PROM programmer. Within minutes you have entered the necessary details and the chip is silently programmed to become the physical reality of your design.

Furthermore, when you progress to more advanced designs you sit at a personal computer running powerful logic design software. The system first verifies your design information by simulating its action, then at your command downloads details to a programmer.

The ICs you use are called Programmable Logic Devices or PLDs for short. They are not fantasy. They are with us now. (Fig.1 and Fig.2).

Fig.2. *Sources of PLD programming information*

Fig.1. *PLD design procedure*

Programmable logic devices are set to make the same impact that microprocessors made in the 1970s. PLDs are not new, they have evolved over the past decade. Now that teething problems of slow switching speed and high power consumption have been solved, their use is becoming widespread in many applications which have required boards full of logic or upon which a microprocessor solution has been used as a sledgehammer.

The range of applications is wide. New types of PLDs are being introduced by the manufacturers to increase their total programming capacity and flexibility. They are rapidly becoming the designer's dream of an uncommitted 'black box' waiting to be programmed to become the circuit the designer requires.

And what if it needs modification as most prototypes do? Well, at the worst the PLD is discarded and a new one programmed. However, erasable PLDs are now available. Like EPROMs, simply expose to ultra-violet light and the device can be reprogrammed.

THE CHOICE OF COMPONENTS

Never before has the electronics designer had so many choices in the type of logic components used to construct circuit (Fig.3).

Since ICs became commercially available small scale integrated (SSI) circuits such as the bipolar 7400 series and the CMOS 4000 series have been used for logic gates and simple sequential logic circuits. Later as integration increased to medium scale integration (MSI) more complex logic such as counters and arithmetic functions became available. These are cheap and easy to use and have been the staple diet of home constructors for many years.

Full custom IC design is still out of the scope of most applications designers. Fully specifying the function, architecture and layout of an integrated circuit for a specific application can be handled only by the largest companies and research organisations with the most advanced equipment. Full custom design is very expensive and only justifiable for high volume manufacture or for military applications.

An area of increased activity is that of semi-custom design. There are two main types. The first is the standard cell where a chip designer using an advanced computer workstation can call areas of previously designed ICs from a library and fit them together as desired. The finished design is then passed to a 'silicon foundry' where the chips are manufactured.

The second type of semi-custom design is the uncommitted logic array or ULA. These comprise arrays of logic gates on silicon chips which are

Fig.3. *Logic IC types*
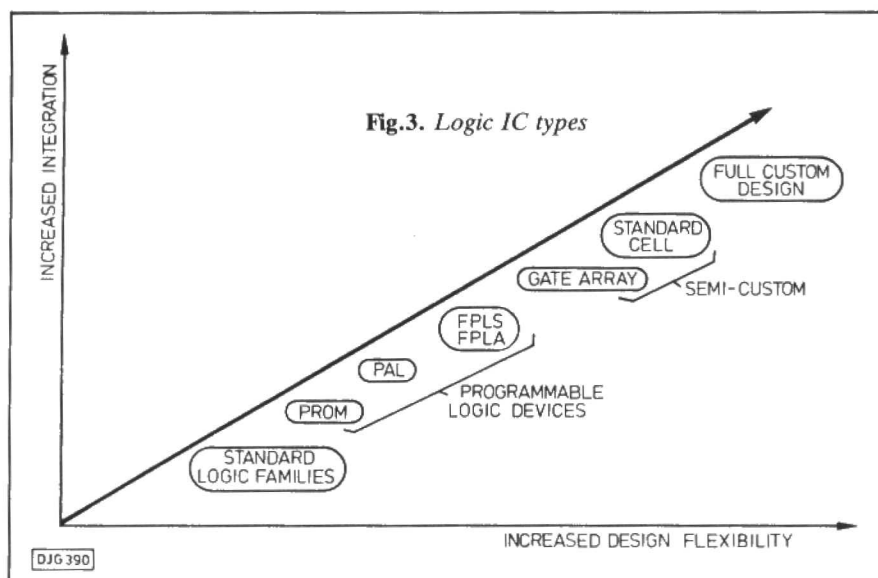
manufactured in bulk by the chip manufacturer except for the final metalisation layer which normally determines the functions of the gates and how the gates are connected. The customer specifies the connections required and a number of ICs are completed with this final mask.

Now this range of choice is widening to include many types of PLDs. Each of these will be described fully in due course, but brief descriptions are introduced here.

Field programmable gate arrays, or FPGAs, are simply arrays of multiple input AND gates. Internal fusible links (Ni-chrome as with PROMS) can be blown or left intact such that the outputs are linked to the inputs through the AND gates. FPGAs can be used for applications such as random logic, address decoders, code detectors and fault monitors.

A manufacturer called Monolithic Memories Incorporated developed programmable array logic devices or PALs, which have an array of programmable AND gates followed by fixed input OR gates. Again these can be used for random logic, code

converters, etc.

Other manufacturers, such as Signetics/Mullard responded with their own types of PLDs, generally known as field programmable logic arrays, FPLAs or just PLAs for short. These have programmable AND arrays and programmable OR arrays, sometimes with registers or bistable latches at the outputs.

Finally we have perhaps the most advanced and flexible type of PLD which is the field programmable logic sequencer OR FPLS. These have programmable AND arrays, programmable OR arrays, internal state registers and external state registers all on one chip! As suggested by the name, FPLSs can be applied to sequential clocked logic functions such as synchronous up/down counters, shift registers, bidirectional data buffers, timing function generators, system controllers and synchronisers, priority encoders and an unlimited number of customised applications.

ADVANTAGES OF PLDs

There are a number of advantages with PLDs over standard logic ICs. Surprisingly, cost of the raw components

is not one of them because they are still relatively expensive, probably more expensive than the combined cost of the standard chips replaced.

However, with reduced design costs through quicker design time and simplified PCB design and construction, the PLDs become competitive. PLD circuits are more reliable because there are fewer soldered connections and for large systems less cooling may be required.

An advantage which may not be immediately apparent is that of smaller stock inventory. A supply of 20 to 30 PLD types could replace the functions of hundreds of SSI and LSI types. When a particular device is required, the appropriate PLD is programmed from one of a library of computer files stored on disk.

The design using a PLD is more secure than with standard chips. Although data sheets give all the relevant details for programming, the actual programmed function is not easily identified without the design details. Copying of circuits is not as easy. Some PALs also have a 'verification disable' function which means that copying is made even harder.

The advantage of circuit security can also be a disadvantage to the maintenance technician. Whereas the functions of standard chips can be checked using logic probes and analysers against data-sheet information, the PLD remains a mystery unless its programmed functions are known.

PLD NOTATION

Each input to a PLD array is spilt into two paths by a true/complement buffer. These are shown in Fig.4. One path feeds the true logic state through fusible links to the array, e.g. logic 1 if logic 1 is applied to the input. The other path is the complement or inversion of the input, e.g. logic 0 if logic 1 is applied to the input.

The gates within PLDs can have many inputs, up to sixteen in some cases. If all the input lines were drawn from the arrays, the diagrams would become
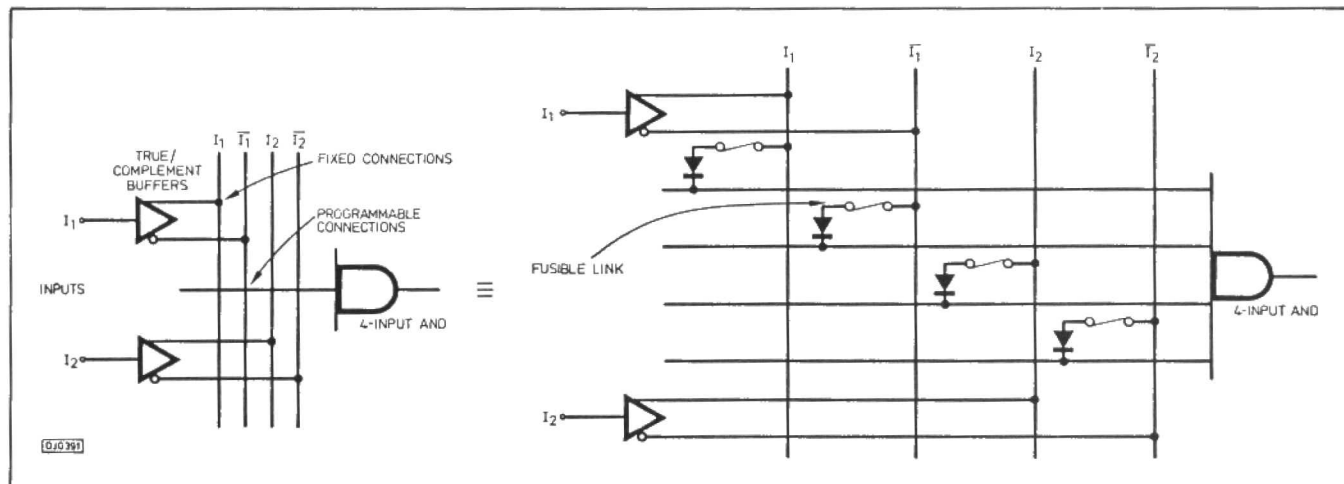
Fig.4. *For simplicity PLD notation shows gates with multiple inputs as a single line*
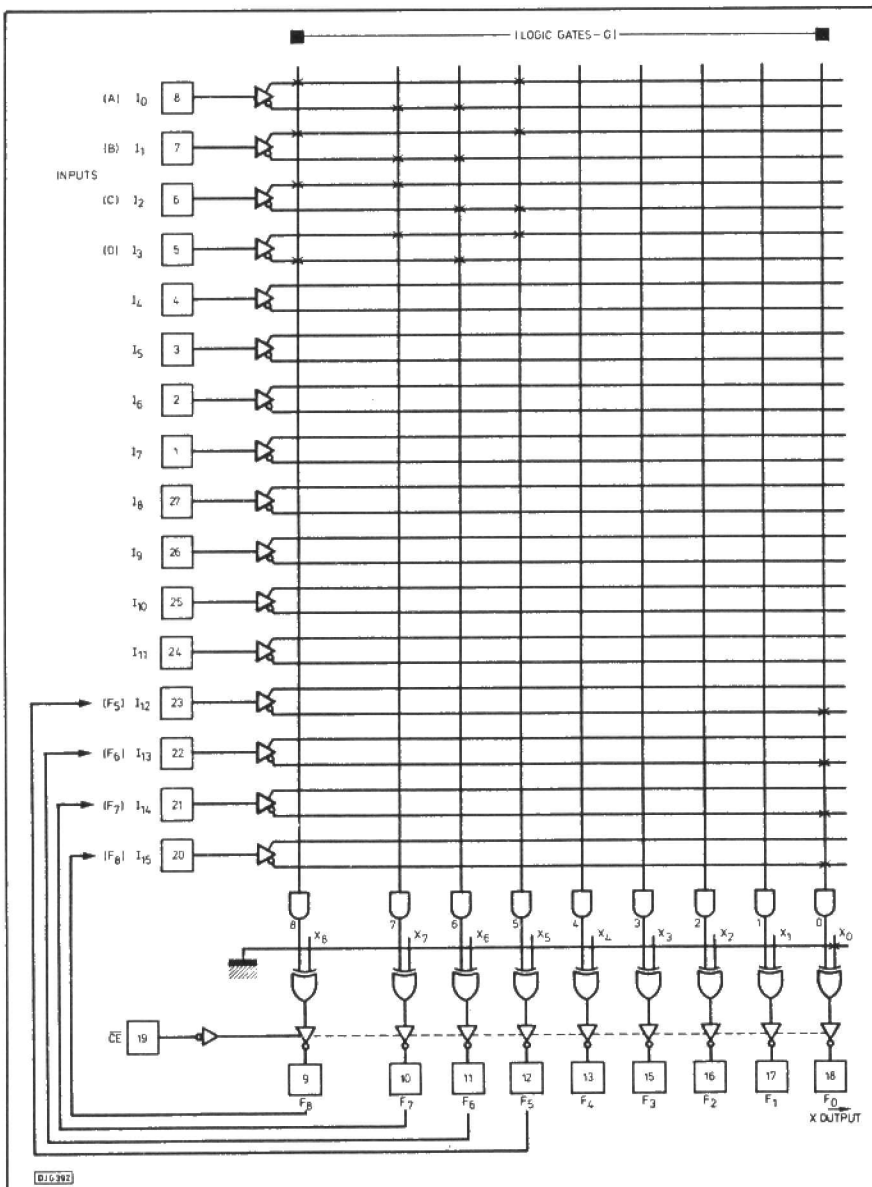
Fig.5. *PLS103 field programmable gate array*

This is applicable to any number of inputs. So by taking the complement from the input buffer and programming the appropriate AND output to be inverted we achieve the equivalent of the OR.

The NOR function is the OR followed by an inversion. This is the same as the AND function with all inputs individually inverted, giving

$$\overline{A.B.C.} = \overline{A} + \overline{B} + \overline{C}$$

A PLS103 programmed to be a mixture of random logic is shown in Fig.7. Note that the AND outputs are fed round to inputs to a programmed OR to give the Boolean relationship:

$$X = \overline{A}BCD + A\overline{B}CD + AB\overline{C}D + ABC\overline{D}$$

The "fuse-map" for this application is shown in Fig.5.

Outputs
$F_5 = \overline{A}.B.C.D$
$F_6 = A.\overline{B}.C.D$
$F_7 = A.B.\overline{C}.D$
$F_8 = A.B.C.\overline{D}$

The outputs F_5 to F_8 are fed back to inputs I_{12} to I_{15} where they are individually complemented and fuse X_0 is left intact giving

$$X = \overline{F_5} . \overline{F_6} . \overline{F_7} . \overline{F_8} = F_5 + F_6 + F_7 + F_8$$

Fig.6. *FPGA OR function*

Fig.7. *PLS 103 random logic application*

ridiculously overcrowded. So a single line is drawn from the array and each intersection has a programmable fuse link which can be left intact or blown as shown in Fig.4.

A TYPICAL FPGA

The PLS103 (shown in Fig.5) is a Mullard/Signetics field programmable gate array with 16 inputs and 9 outputs.

Each input has a true/complement (T/C) buffer which applies the true state of the input to one row of the array and the complement (or logical inverse) to another row. Each row from a T/C buffer can feed the signal down a line to a multiple input AND gate depending on whether the appropriate fuse link is left intact or blown.

If all the lines connecting to the AND gate were shown, the diagram would become excessively overcrowded. Therefore only a single line is shown to the AND gate, crossing all the true and complement input lines. A cross indicates that the appropriate fuse is intact,

i.e. still electrically connected. The absences of a cross indicates that the fuse has been blown.

Each output of the PLS103 can be programmed active-high (ie a non-inverted output) or active-low (an inverted output) by the X fuses at the exclusive OR gates. Because of the inverting output buffers, a blown X fuse give a true F output and an intact X fuse gives the inverse. In this way the AND or NAND functions are achieved.

The chip enable (CE) makes the output buffers active when CE is made logic 0. The outputs are high impedance when CE is made logic 1.

Logic functions other than AND can be programmed into the FPGA. For example, as shown in Fig.6, the OR function is derived from DeMorgan's Law. This simply states that if the individual inputs of a NAND gate are inverted, the overall function is OR, giving

$$\overline{A.B.C.} = A+B+C$$

Fig.8. *PROM as a PLD*

PROMS AS PLDS

A programmable read only memory (PROM) as shown in Fig.8 is really a simple PLD. The internal structure can be considered as a fixed AND array which is normally used to address memory locations, followed by a programmable OR array which stores binary information by the fuses either blown or left intact.

This fixed-AND/programmable-OR format can be used to program Boolean logic functions between the inputs and outputs. By allocating the PROM address lines as variable inputs, and the data lines as individual outputs, a truth table can be compiled to specify the system conditions.

Fig.9 and Table 1 show an example of a PROM programmed as a binary coded decimal (BCD) to seven segment display (SSD) decoder.
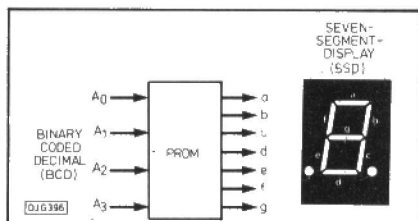
Fig.9. *PROM used as a BCD to SSD decoder*

	A_3 A_2 A_1 A_0	g	f	e	d	c	b	a
0	0 0 0 0	0	1	1	1	1	1	1
1	0 0 0 1	0	0	0	0	1	1	0
2	0 0 1 0	1	0	1	1	0	1	1
3	0 0 1 1	1	0	0	1	1	1	1
4	0 1 0 0	1	1	0	0	1	1	0
5	0 1 0 1	1	1	0	0	1	1	0
6	0 1 1 0	1	1	1	1	1	0	1
7	0 1 1 1	0	0	0	0	1	1	1
8	1 0 0 0	1	1	1	1	1	1	1
9	1 0 0 1	1	1	0	1	1	1	1

Table 1 Binary Coded Decimal to seven-segment decoder.

PROMs can be programmed only once, so the designer needs to be sure of his design before committing it permanently. For development work, EPROMs can also be used so that any modification could be achieved by erasing then re-programming the device.

There are two main disadvantages with PROMs used as PLDs. First, large areas of the OR array may be unused, especially if a large number of inputs are required with only a few Boolean terms (the total OR array doubles for each additional input/address line). The second drawback is that PROMs and EPROMs are relatively slow. **PE**

from Unisat, a joint venture between British Telecom, British Aerospace and GEC Marconi. Unisat's price spiralled, the company's spokesman did a wonderful job of alienating the press and the BBC opted out.

When the Home Office told the IBA it could grant a 15 year franchise, there was no longer a buy-British obligation. In December 1986 the IBA gave the DBS franchise to BSB, a consortium of Amstrad, the Granada and Anglia TV groups, Pearson publishers and Virgin, with support from Independent Television News. Since then BSB has been trying to raise £600 million. Perhaps smelling disaster, Amstrad backed out.

The big problem is Astra. Société Europeane des Satellites of Luxembourg will launch a rival direct broadcasting satellite called Astra 18 months ahead of BSB. Astra will have 16 channels compared to BSB's three. Astra will broadcast with 45 watts of power, compared to BSB's 110 watts, but this is just strong enough to receive with dishes less than 90 cm in diameter. And dishes less than 90 cm need no local government planning permission.

Most worrying for BSB, Astra will be at 19 degrees East, whereas the UK slot for BSB is at 31 degrees West. Once viewers have pointed their aerials at Astra, they will not be able to receive BSB without a motor drive.

BAe offered to let BSB defer payment of £30 million for 5 years. But BSB wanted £60 m. BAe, seeing the risk of a massive loss on an unsecured debt, said no. More important for BSB, BAe was unable to guarantee a launch rocket and insurance against the rocket failure and satellite loss. Hughes could, because the US company has a deal with McDonnell Douglas which guarantees a launch in autumn 1989 on a Delta rocket, with insurance against failures.

Both Gill and Sapper admitted that they are not interested in success of the BSB venture unless BAe is involved. Sapper says he does not believe DBS will create jobs anyway, even for programme pro-ducers. "Only the money markets want DBS" he says. "Holding technology and patents does not create jobs". Gill says he "couldn't care less about DBS if there is no industry involvement".

Neither seemed interested in the jobs in Mullard that will come from making the chip set needed to receive the new format MAC signals which BSB will transmit. And although BAe will certainly lose design and assembly work, the Stevenage company's "British" satellite would be 60% or 70% foreign anyway. The electronics and even some of the metalwork has to be bought in from abroad. **PE**
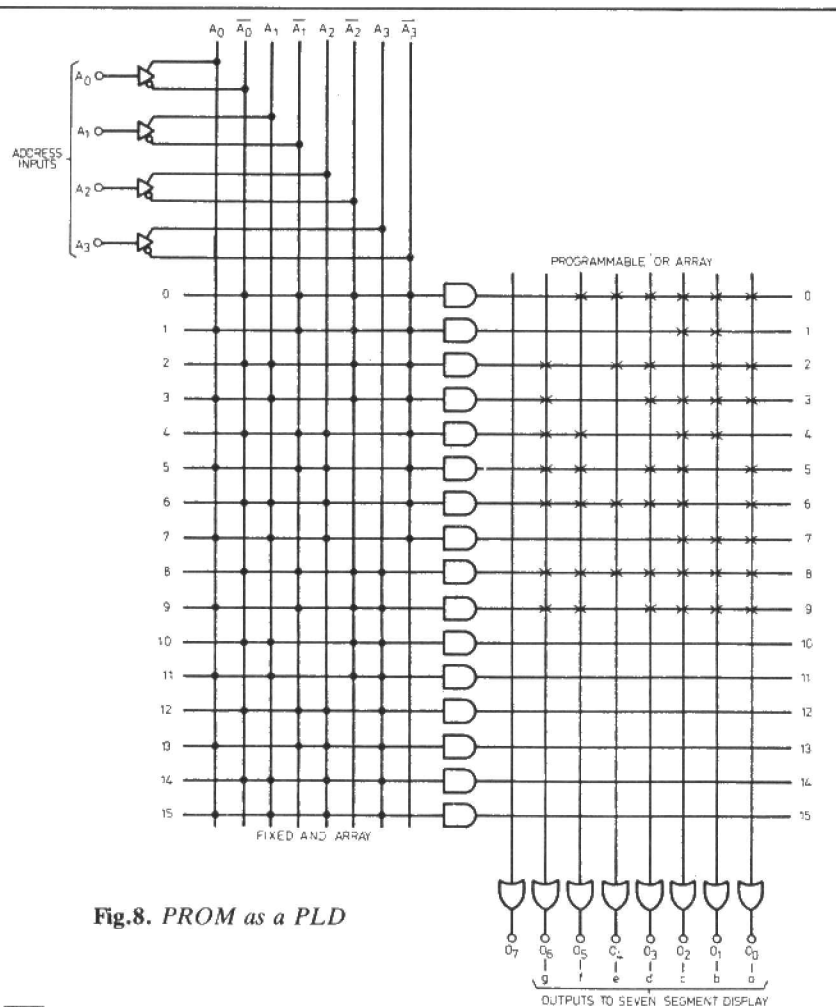
While error correction on up-to-date devices like Compact Discs can be quite spectacular, good old analogue vinyl has to search for lower-tech solutions.

CLICK ELIMINATORS
BY THE PROF
Just scratching the surface

PULSE BLANKERS are in various types of equipment, but are perhaps most frequently encountered in up-market radio receivers. This mainly means communications receivers, but also some car radios and hi-fi f.m. tuners (where they are used to combat car ignition noise). Technically, noise blanking in radio receivers tends to be relatively easy and is often quite effective. Special noise blanker chips for radio applications are available. Pulse blanking is something that can be applied to audio signals, but it tends to be much more difficult to apply at these much lower frequencies. It is also much more difficult to produce a glitch-free out put. This glitch problem is due to the generally longer blanking pulse durations needed in audio applications.

What we are really talking here are the so called "click eliminators" used to process the output from conventional disc recordings. Most designs of this type successfully remove the noise pulses produced by scratches on the record, but the few milliseconds of blanked signal often results in an audible glitch. A gap of around 10 milliseconds or more is needed in order to produce a gap in the signal that is audible as such, which is about three times longer than the blanking period required in this application. The glitch sounds rather like a tape "drop-out" in a cassette tape system. Although swopping a "click" for a "drop-out" might seem like "out of the frying pan and into the fire", the "drop-out" is quite definitely the lesser of the two evils. In fact the glitch is quite noticeable sometimes, but not apparent at all on the other occasions. This seems to depend on the nature of the programme signal, and exactly where in it the noise pulses occur. In general, the "clicks" are most noticeable during quiet passages, and it is during this that the blanking can be most effective.

UP TO SCRATCH

In this Experimental Electronics article we will take a look at the techniques involved in "click elimminators", with some practical circuits for you to try out. I will not claim that these circuits can transform a badly stratched record into one that has compact disc performance. What they can do is to render a badly scratched record worth listening to again. With many great recordings of the past never

likely to be reissued, if you have some prized but old and damaged disc recordings, a unit of this type offers a means of getting some more mileage from them.

One point that has to be made at this stage is that these circuits are not intended to operate with the direct output from a cartridge. They must be fed from the pick-up by way of a suitable preamplifier, which should provide an output of around 2 volts peak from a resonable low source impedance. As countless circuits for preamplifiers of this type have been published over the years, a suitable design will not be considered here.

Fig.1. *Block diagram for a basic noise blanker*

A basic noise blanker is not particularly complex, and the arrangement shown in Fig.1 is about the most simple scheme that will work. The top row of blocks are the signal handling stages, and the first of these is a lowpass filter. The purpose of this is to give a slight delay so that the blanking action can take prior to the landing edge of the "click" signal reaching a significant amplitude. This circuit can also be used to give a conventional scratch filter action. It is important to realise that scratch filters and blankers are very different in their methods of operation. A blanker is effectively cutting out the noise spikes caused by a bad scratch, whereas filters just provide simple top-cut filtering (above about 7kHz). This filtering is effective against small scratches which only generate high frequencies, but has little effect with severe scratches. These often produce frequencies well down into the middle audio range. This makes simple filtering an impractical way of counteracting them. Of course, it could be that the record is not infested with minor scratches and that the scratch filtering is not needed. With the circuits I have tried

results have only been worthwhile if a certain amount of treble cut has been introduced, and it would seem that with this simple type of blanker circuit some loss of audio quality has to be tolerated.

The next two stages are an analogue gate and a "hold" circuit. The gate is momentarily switched off to block the noise spikes from the output, and the hold circuit maintains the output voltage while the signal path is blocked. This gives a blanking action of the type shown in Fig.2, where waveform (a) represents the input signal, and (b) is the resultant blanked output signal. Obviously the output signal deviates from the original (non-scratched) signal, but this short period of silence is a much more minor error than that obtained with the noise spikes left unprocessed. Although in Fig.2 the noise spikes are shown as having a peak amplitude not much in excess of the amplitude of the main signal, in practice the noise spikes will often be 20dB or more higher in level. In fact the difference can be as much as 60dB or so if a bad scratch occurs during a quiet passage (which they normally do!).

The gate must be switched to block the signal at the appropriate times, and this is the job of the highpass filter and the monostable. Some means of differentiating between the noise spikes and the main signal is needed, and there is more than one valid approach to this problem. These mostly rely on the fact that the rise time of a noise spike is faster than that of a normal signal. Highpass filtering is an effective way of extracting the noise spikes, which tend to have strong high frequency components. Provided the pick-up and stylus are good quality types, strong signals above the upper limit of the audio range will be present, and it is these that are used to trigger the monostable. The monostable
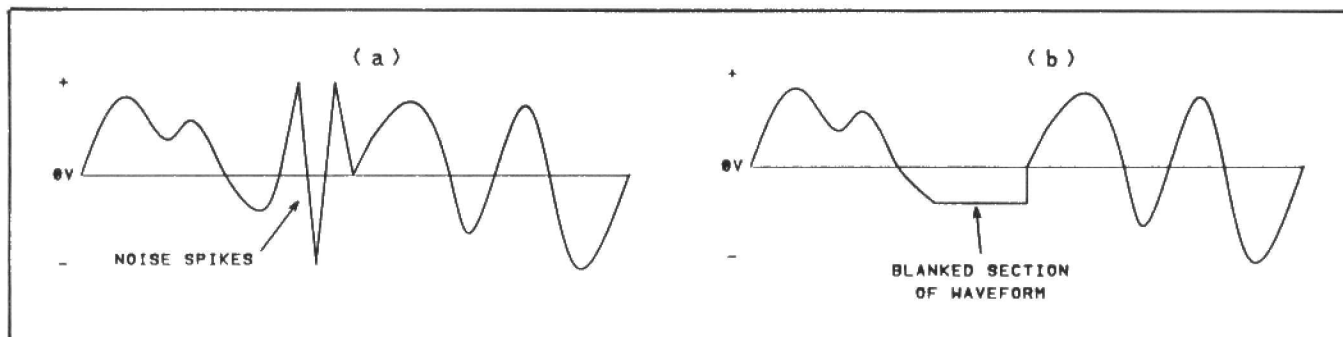
Fig.2. *Using a blanking action to remove noise spikes*

controls the duration of the blanking period, and this must be long enough to fully cover each burst of noise spikes. In practice a duration of about 3.5 milliseconds seems to be sufficient.

BLANKING ON IT

It is easy enough to knock-up a simple blanker of the type outlined in Fig.1, but the chances of it working well are very slight (probably nil)! Under ideal conditions it could in fact work quite well, but in reality there is no point in banking on the signal always being co-operative. The two principal problems are spurious triggering and always getting the unit to trigger before the noise spike has risen to a significant amplitude.

Fig.3 shows the block diagram for my initial "click" eliminator design, which largely overcomes both problems. It resembles the original set up of Fig.1, but has obviously been expanded somewhat. The stages in the main signal path are actually much the same as before, but a buffer amplifier has been added at the input to ensure that the lowpass filter is driven from a suitably low source impedance. At the output some further lowpass filtering has been used, and this circuit also provides the "hold" function.

The most important changes are in the control circuits for the analogue gate. The single highpass filter has been replaced by two filters plus a variable gain amplifier. Two stages of filtering (both third order types) gives good attenuation of audio frequency signals and helps to avoid spurious triggering when the volume of the main signal is high. The amplifier ensures that the circuit has adequate sensitivity, and the variable gain enables the sensitivity to be adjusted for optimum results.

With the original arrangement the unit would trigger on either negative going noise spikes, or positive going types, but not both. Just which type would trigger the unit is dependent on the type of monostable used. If the leading edge of the noise signal happened to be of the wrong polarity, the gate would not block the signal until the initial half cycle of the noise signal had passed. The practical result of this would be that the unit would only be effective on about 50% of the "clicks" it processed. In the improved design the output from the second highpass filter is fed to a window discriminator. This detects when the signal strays outside certain voltage limits, and is activated by the signal going either positive or negative by more than a certain amount. The unit therefore responds equally fast to leading edges of either polarity.

A simple pulse shaper is used at the output of the window discriminator to produce an output signal that will trigger the monostable reliably. In fact there are two monostables in this version of the unit, one of which drives the gate circuit,

as before. The control input of the gate is driven via an inverter, otherwise the effect of the unit is to pass the "clicks" and block the main signal.

The second monostable provides a longer output pulse of around a second in duration, and its output connects back to the pulse shaper circuit. Its effect is to block any further blanking pulses for the duration of its output pulse. This is really just a safety measure in case the highpass filters should fail to prevent strong high frequency components in the main signal from activating the unit. This could potentially cause large sections of the programme material to be blanked out, although this could only occur in an extreme case. The additional monostable ensures that the unit can only be activated about once per second even under worse case conditions, which should prevent any severe corruption of the signal.

There is a drawback in this system in that of two scratches following closely one after the other, the second one will not be processed. However, the pulse duration of the second monostable could be shortened slightly if necessary in order to accommodate this eventuality. There would be no difficulty in making its pulse duration adjustable, or in having several switched pulse lengths. An alternative system which can work very well is to have a sort of a.g.c. (automatic gain control) system. The idea here is to have the sensitivity of the
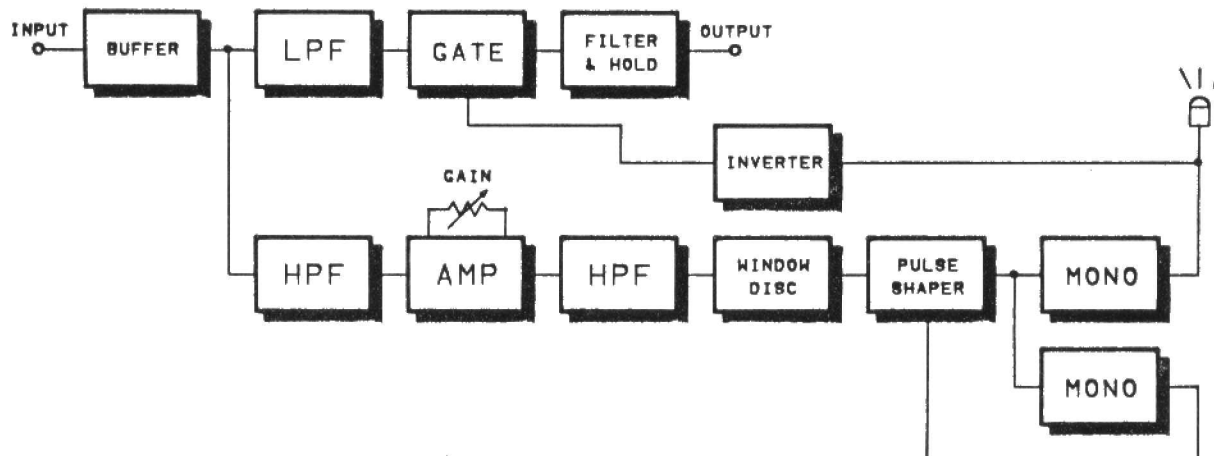

Fig.3. *Block diagram for a practical "Click" Eliminator*
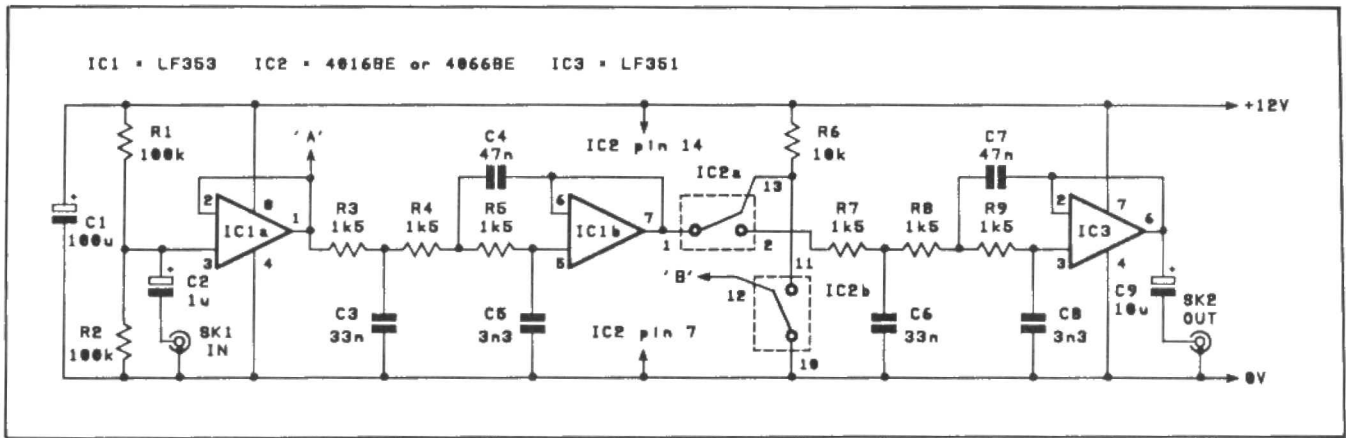
Fig.4. *The circuit diagram for the signal processing stage*

trigger circuit reduce somewhat at high input levels. Unwanted triggering did not seem to be a very great problem with this design, and I decided to settle for the simpler solution of the extra monostable. The a.g.c. approach would be an interesting one to follow up for anyone who would like to try developing the circuit for the ultimate in performance.

CIRCUITS

The circuit of my initial "click" eliminator design is shown in Fig.4 (the signal processing stages) and Fig.5 (control pulse generator stages).

Taking the signal processing stages first, IC1a is the input buffer stage and it provides an input impedance of about 50k. This is followed by a conventional third order (18dB per octave) lowpass filter based on IC1b. This has a cutoff frequency of just over 7kHz. This is followed by the analogue gate, which is a CMOS bilateral switch. I tried both the 4016BE and the pin compatible

4066BE types, and there seems to be no significant difference between the two in this circuit. They are both quad SPST switches, but in this case only two switches are used: one as the gate (IC2a) and one as the inverter which drives the gate's control input (IC2b). The other two switches are just ignored, although in a stereo unit these could be used in the second stereo channel. Another third order lowpass filter having a 7kHz cutoff frequency is used at the output of the unit. This is based on a bifet operational amplifier (IC3) which has an extremely high input resistance of around one million megohms. Thus, during the blanking periods, the charges on the filter capacitors do not have a chance to degrade significantly, and the required "hold" action is provided. Due to the shortness of the blanking periods a high input resistance device is probably not essential for the IC3 position, but I felt it was best to play safe and use a f.e.t. input device here.

IC4a acts as the buffer amplifier in

the first highpass filter stage, which is another third order type. Its cutoff frequency is at approximately 20kHz. IC4b is the voltage amplifier, and this is a simple non-inverting type. Its voltage gain can be varied from unity to about eleven times by means of VR1. This stage is followed by another third order highpass filter having a 20kHz cutoff frequency.

IC6a and IC6b act as the window discriminator, with D1, D2, and R21 acting as a simple gate to combine their outputs. The output goes low when the input voltage strays outside the window limits. This negative going signal is coupled by C18 to the trigger inputs of two 555 monostable circuits (IC7 and IC8). Both devices are actually TLC555Ps, which are low power 555s. In this application it is not the lower current consumption of these devices that are of primary importance. The standard 555 tends to put noise spikes on the supply lines as it "crowbars" the supply on output transitions. In the

Fig.5. *The blanking pulse generator stage*

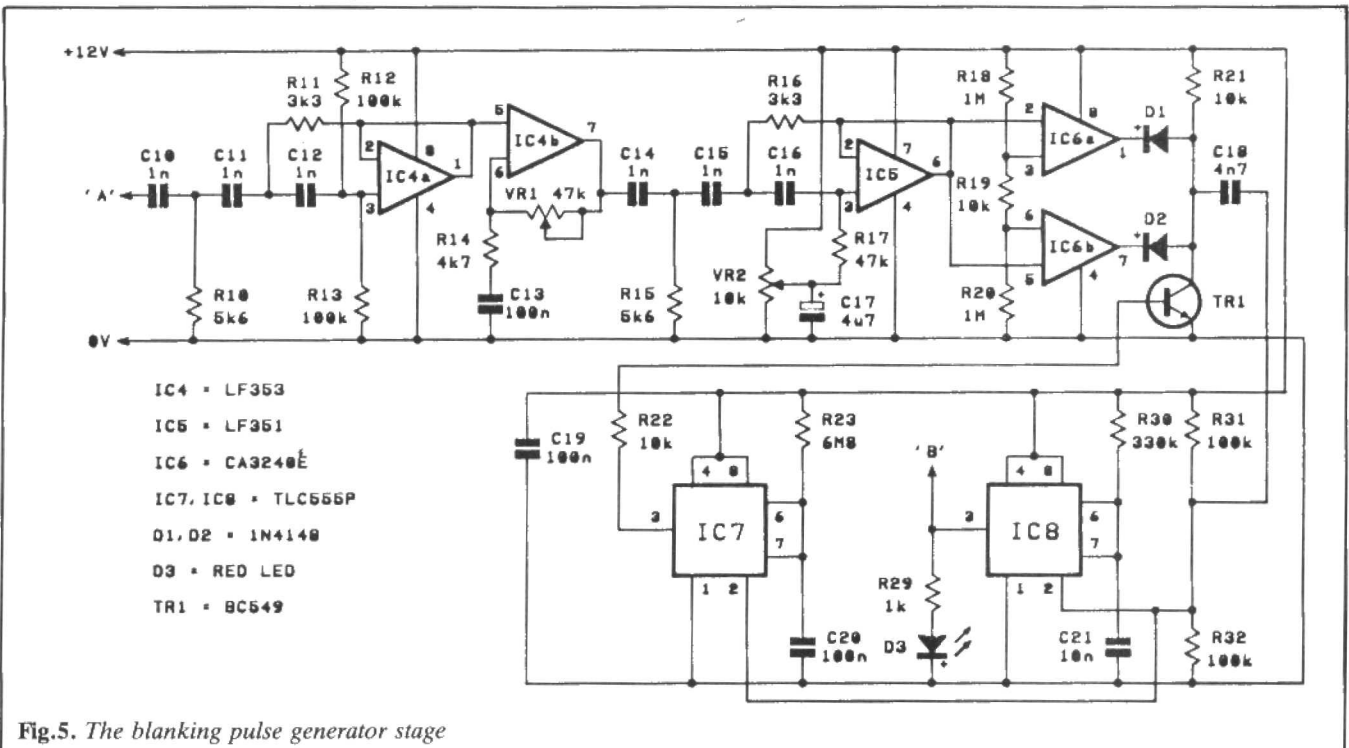current context this could result in the circuit eliminating the "clicks" caused by scratches but inserting its own noise spikes from the monostables! Using low power 555s avoids this problem.

IC8 generates the shorter pulse (about 3.5 milliseconds) which is fed to the gate circuit. Its output also drives l.e.d. indicator D3, which therefore flashes briefly each time the unit is triggered. This feature is very useful when initially setting up and testing the unit. IC7 generates the longer pulse, which is about 750 milliseconds in duration with the specified timing component values. The pulse duration can easily be changed, and it is proportional to the values of R23 and C20. The output from IC7 is used to drive common emitter switching transistor TR1. When switched on, TR1 holds the output of the window discriminator in the low state, preventing any negative transitions which could trigger IC8 again.

back it off any further than is really necessary though, as this could reduce the effectiveness of the unit. The 12 volt supply for the unit must be a very low noise type if good results are to be obtained.

In use the unit certainly provides a very worthwhile improvement, and in many cases leaves little or no audible glitch. It seems to be less than 100% reliable though, and sometimes leaves a very noticeable "click" on the output signal. Just why some "clicks" should be effectively combatted while others are not detected in time is not entirely clear. Presumably some "click" signals have a relatively slow initial rise time so that they are not detected early enough. Lowering the cut-off frequency of the highpass filters or increasing the voltage gain of the amplifier stage would improve reliability in this respect, but would leave the unit more open to problems with spurious triggering.

the risk of spurious triggering. When I first tried circuits of this type (which was over ten years ago) analogue delay line chips were quite expensive and there was plenty of incentive to find a successful circuit that did not require them. Things are very different these days, and "bucket brigade" chips, although not a matter of pence each, are not all that expensive. Certainly resorting to one of these will not vastly increase the overall cost of the unit.

Fig.6 shows the circuit diagram for signal processing stages based on a delay line. This circuit is designed to replace the one of Fig.4 in the original design, and must be used in conjunction with the circuit of Fig.5 to produce a complete "click" eliminator unit.

The delay line chip is the Hitachi MN3004 512 stage PMOS type (IC2). This is used with its matching MN3101 clock chip (IC3). Apart from providing a two-phase clock signal, IC3 also
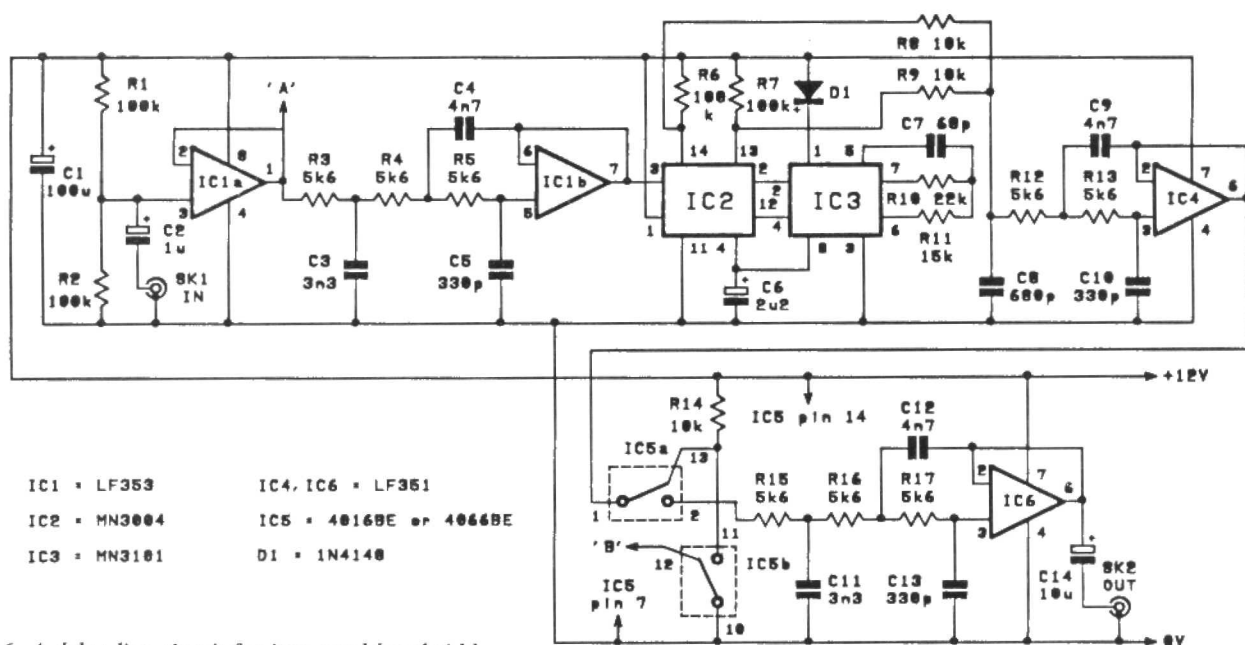
Fig.6. *A delay line circuit for improved bandwidth and reliability*

RECORD RESULTS

Before the unit will function properly VR2 must be given the correct setting. This control sets the quiescent bias level on the input signal to the window discriminator, and this bias level must be at roughly the middle of the window voltage range. If VR2 is adjusted backwards and forwards around the middle of its adjustment range, it should be found that D3 flashes on as VR2 is taken past a certain setting. This setting is approximately the right one, but VR2 can be fine tuned in use to optimise results. Ideally VR1 would be set at maximum sensitivity (maximum value), but if this is done the unit might be oversensitive, with frequent triggering. If this should be the case, VR1 must be backed-off far enough to prevent frequent unwanted triggering of the unit. Do not

DELAY LINE

Performance can be greatly improved by using an analogue ("bucket brigade") delay line in place of the lowpass filter of the original design. This brings two advantages. One is that the delay line can give the full audio bandwidth if desired, and the other is that it gives far greater reliability. Even a fairly short delay time of around 1 millisecond, which is easily achieved with even one of the smaller delay line chips, gives ample time for the gate control circuit to operate and cut off the signal. The gate is actually activated before the noise signal reaches it, rather than early on the wave front. Because it is unnecessary to detect the noise spikes very early on the initial half cycle, good results can be obtained using relatively low sensitivity in the pulse detector circuit. This reduces

provides a bias voltage needed by IC2. The clock frequency is quite high at around 100kHz, which gives a delay of only about 2.5 milliseconds. A high clock frequency has the advantage of placing lesser demands on the input and output filters, and it also enables a wider bandwidth to be obtained. A delay of around 2.5 milliseconds is actually somewhat more than is really needed in this application, and the clock frequency could be pushed even higher by reducing the values of R10, R11, and C7. However, trying to raise the clock frequency much above its current level could result in the circuit malfunctioning. Also, the MN3004 data sheet would seem to suggest that a higher clock frequency will significantly degrade distortion performance. Note that R30 in Fig.6 might need to be made somewhat higher in

value (say about 470k) in order to elongate the blanking pulse. This compensates for the fact that the blanking pulse commences earlier, and could therefore finish before the end of the noise signal unless it is slightly lengthened.

At the input of the unit there is a buffer stage and a third order lowpass filter, much as in the original design. However, the cutoff frequency of the filter has been made higher at around 20kHz, and the circuit provides no significant top-cut filtering. Another third order filter having a 20kHz cutoff frequency is used at the output of the unit, and this removes the stepping on the output waveform. This circuit feeds into the gate circuit, which is identical to the one in the original design. The analogue gate is followed by the filter and hold circuit, which is again much the same as the original circuit, but the cutoff frequency has been raised to about 20kHz.

Although noise reduction systems are often used with delay line circuits, there is no need for any processing of this type with the present design. With short delay times most delay line chips provide an excellent signal to noise ratio, and the MN3004 has a very respectable signal to noise ratio of around 80 to 90dB. It also offers low distortion levels that are generally below 1%. R1 and R2 could be replaced with a 220k preset potentiometer to enable the biasing to be adjusted for optimum distortion performance, but the MN3004 provides so much "headroom" that there seems to be little advantage in doing this.

Results with the delay line version of the blanker seem significantly improved, and the additional expense and complexity of this version seem to be well justified. The unit always triggers in time and provides a proper blanking action.

STEREO

As described so far the blanker is only suitable for monophonic use. One way of obtaining stereo operation is to simply built up two units and to use one in each stereo channel. This is not the normal method with stereo blanker circuits, and it is more usual to blank both channels together. Separate signal processing stages are still needed, but this simplifies things slightly by enabling a single control pulse generator to be used. The control pulse generator circuit is well able to drive two gate circuits without the need for any buffering, but some form of mixer is needed at the input so that it can be fed with the signals from both channels.

A simple two resistor passive mixer might do the job, but it would introduce losses that could degrade performance unless the gain of the voltage amplifier was increased to compensate for them. Better results can be obtained using an active mixer circuit that mixes the two

signals in anti-phase. This might seem to be a good way of preventing the unit from working at all, with the noise signals tending to cancel out one another to give zero output. In practice things do not operate in this way.

Taking the main signal first, some signals are predominantly in one channel or the other, and will be fed straight through to the output with little or no cancelling effect. Signals at the centre of the sound stage are produced by in-phase signals at similar levels in both channels. These do tend to cancel out each other, giving a greatly reduced output level. This helps to attenuate the main signal and reduce the risk of unwanted triggering. The scratch signals will sometimes be predominantly in one channel, and will be fed through to the output having undergone little change. Scratch signals in both channels, so the theory has it, will be mainly out-of-phase and will add together at the mixer to give a stronger output signal. The effect of this type of mixing is therefore to attenuate the main signal, boost the scratch signal, and thus improve the discrimination between the two.

Fig.7. *The mixer circuit for stereo operation*

The simple circuit of Fig.7 gives the required anti-phase mixing action. This just consists of a summing mode mixer circuit with a unity gain inverting amplifier added ahead of one input. VR1 is adjusted to minimise the output level from the circuit with a scratch-free input applied to the unit.

The theory seems to be borne out in practice, and a stereo version of the unit incorporating this mixer seemed to work very well.

DEVELOPMENTS

While this scratch blanker seems to give a very worthwhile improvement when used with badly scratched records, it does still leave a slight audible glitch on most occasions. I suppose that in terms of dB of attenuation the improvement is very large, but human hearing is very sensitive and any slight imperfections tend to be clearly audible. This makes it very difficult to process a scratched record to the point where it

really sounds as if it has been newly pressed. This design is less than perfect, but it is at least as good as any other scratch blanker design I have heard in operation.

Perhaps the best route for further development would be to try adding a zero crossing facility to the gating circuit. By having the gate switch on and off as the signal passes through the zero volt level the slight glitch as the gate switches back on could be avoided. The waveform diagram of Fig.2(b) shows what I mean. The "held" voltage is well negative of the zero volt level, but when the blanking period ends the signal is at roughly the 0 volt level. The signal therefore switches abruptly from its "held" level to the current signal level. It is probably this rapid switching that generates the audible glitches. Sometimes the difference between the two signal levels will only be very small, giving no significant glitch. On other occasions the difference will be very large, giving a very noticeable glitch.

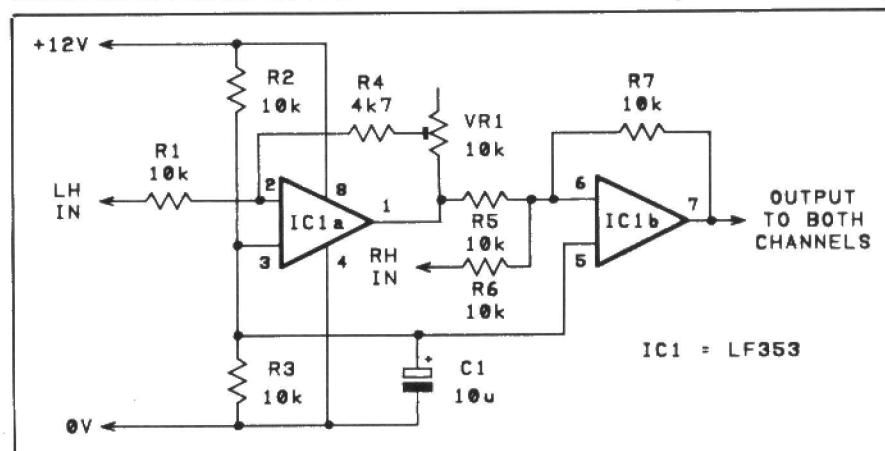Zero point switching would avoid this switching transient altogether, and should therefore provide consistently good results. There is a possible problem in that the blanking period could be extended to the point where a definite gap would be heard in the signal. This might be preferable to the scratch pulses, but could be avoided by having a "time-out" facility which would not let the blanking pulse go beyond a certain duration. What might be a better way of tackling the switching would be to have the signal gated off immediately, as in the present design, but to then wait until the signal returned to this level again before ending the blanking pulse. This could give generally shorter blanking periods, but the "time-out" facility would still be required as occasionally the signal might not return to the "held" level for some considerable period of time! There is obviously plenty of scope for experimentation and further development here, and I hope to return to this subject at a later date, perhaps with a full constructional project. **PE**
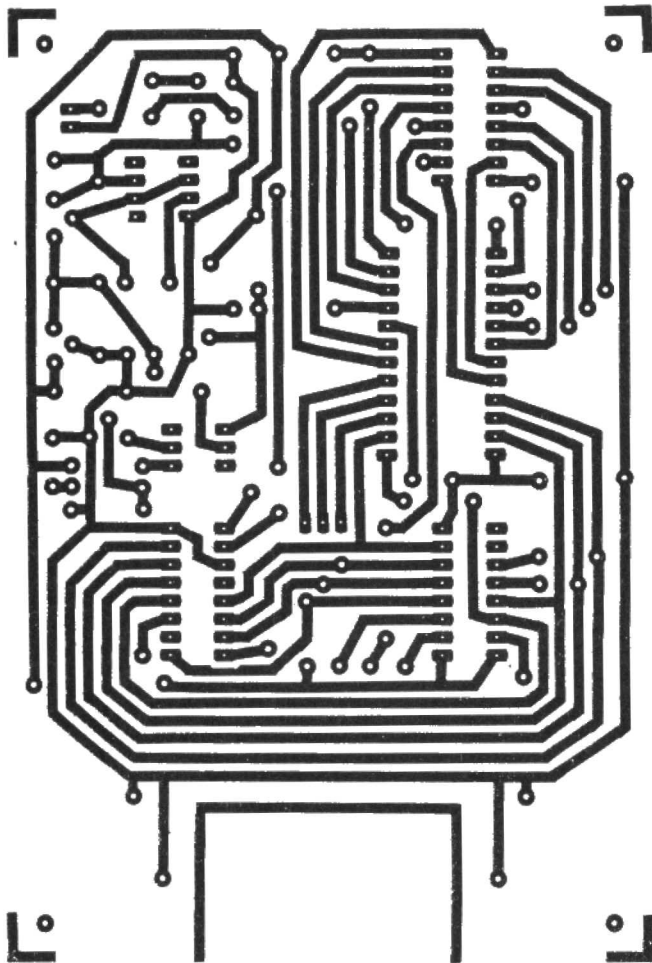
EPROM PROGRAMMER
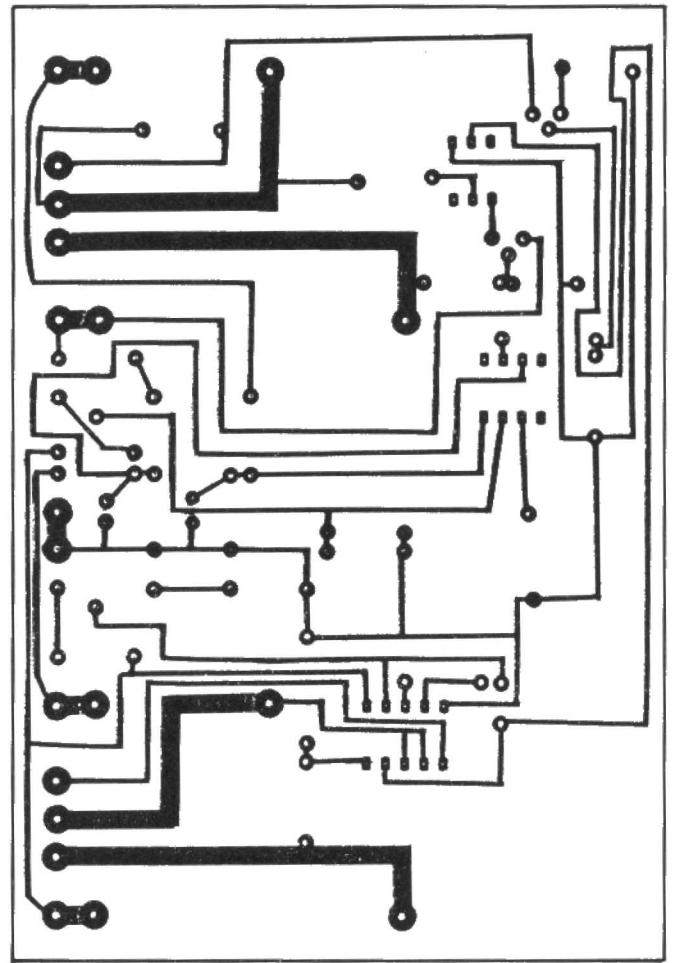
POWER SUPPLY PE 156

TEACHER LOCKER PE 155

GUITAR TO SYNTH PE 157A

HOW TO USE THESE TRACKS

PE 157B

FIRST MAKE TRANSPARENT COPY

(We regret that we cannot supply transparent copies of PCB track layouts.)

STUDIO COPY METHOD

Ask local photographic studio to produce high contrast 1 to 1 positive transparency.

HOME PHOTOGRAPHY METHOD

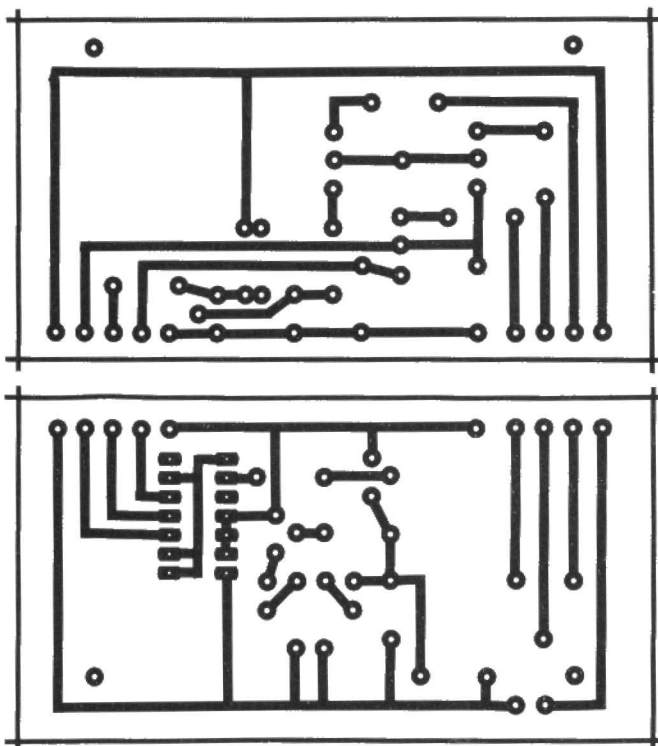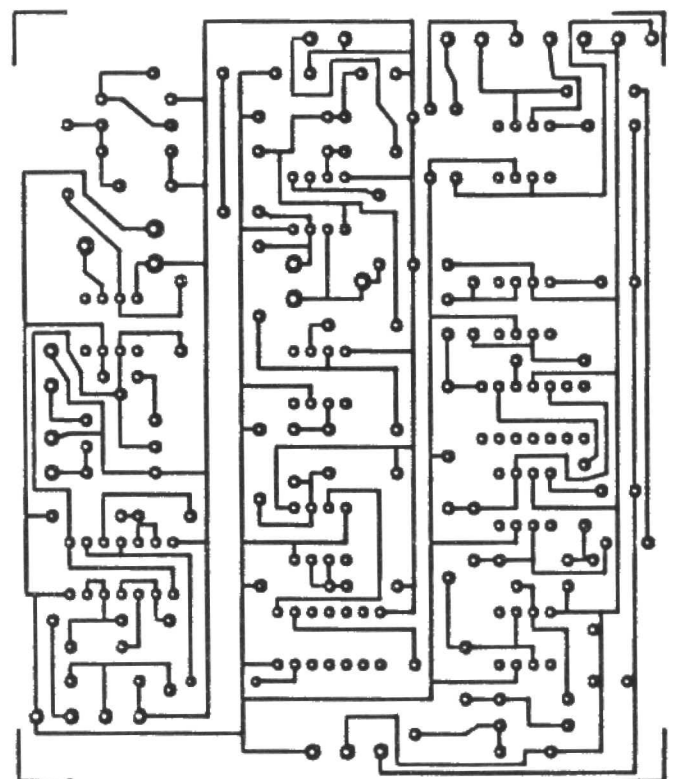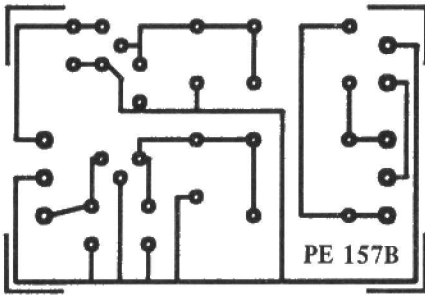Using even, bright illumination, photograph track onto fine grain black and white negative film. Develop film for high contrast. Photographically enlarge image up to lifesize, and print onto high contrast lithographic cut film, such as Agfa Copyline HDU 3P Type 2. Develop in Agfa Litex G90T litho developer, or similar.

PHOTOCOPY METHOD

Ask local photocopy shop to make a good contrast copy onto acetate film. (Some copiers are better than others – shop around.) Then touch up tracks with dense black ink, or photographic opaque ink.

ISODRAFT METHOD

Have a normal photocopy made, ensuring good dense black image. Spray ISOdraft Transparentiser onto copy in accordance with supplied instructions. **ISOdraft** is available from **Cannon & Wrin,** 68 High Street, Chislehurst, Kent. Tel: 01-476 0935.

PAINSTAKING METHODS

Draw image by hand onto clear film or drafting film using dense black ink. Draw direct onto copper surface of PCB fibreglass, using etch-resist inking pen. Use etch resist PCB tracks and pads, taping direct to copper surface, or onto drafting film.

NEXT PRINT ONTO PCB

Place positive transparency onto photosensitised copper clad fibre glass, cover with glass to ensure full contact. Expose to Ultraviolet light for several minutes (experiment to find correct time – depends on UV intensity).

Develop PCB in Sodium Hydroxide (available from chemists) until clean track image is seen, wash in warm running water. Etch in hot Ferric Chloride, frequently withdrawing PCB to allow exposure to air. Wash PCB in running water, dry, and drill holes, normally using a 1mm drill bit.
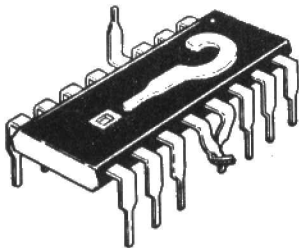
(PCB materials and chemicals are available from several sources – study advertisements.)

* CAUTION – ENSURE THAT UV LIGHT DOES NOT SHINE INTO YOUR EYES. PROTECT HANDS WITH RUBBER GLOVES WHEN USING CHEMICALS.

ALTERNATIVE METHOD

Buy your PCB ready made through the PE PCB SERVICE, most are usually available – see page 60.   PE

Some of the chips from this month's circuits have been chopped and their pins jumbled. Can you name the chips chosen?

Also tell me which features or projects in this month's issue you found most interesting, and which you found least interesting – state as many as you like.

Answers to the editorial office to arrive before the publication date of the next issue. The first three senders of the correct chip identity answers will receive 12 month's free subscription to PE. Where there is ambiguity through chips having identical pin-outs, either answer is acceptable.

First 50 entrants wil receive a valuable set of CMOS pin data references.

Answer and another CHIPCHOP puzzle next month. The Editor's decision is final.

Follow the series and collect the data!

CHIPCHOP – PUZZLE NO 1 TEST YOUR LOGICAL RESEARCH ABILITY AND WIN 12 MONTH'S SUBSCRIPTION TO PE

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CHIPCHOP PUZZLE 1

ALLOCATE THESE PIN FUNCTIONS AND NAME THE CHIPS

+IN,+IN,+INA,+INA,+INB,+INB,+V,+V,+V,+V,+VA,+VB,-IN,-IN,-INA,-INA,-INB,-INB,
-V,-V,-V,-V,BAL,BAL,BALA,BALA,BALB,BALB,CLOCK,CP1,CP2,CTRL,CTRL1,CTRL2,
CTRL3,CTRL4,CURRENT LIMIT,CURRENT SENSE,DATA,DISCHARGE,ENABLE,FREQ COMP,GND,
IN1,IN1A,IN1A,IN1B,IN1B,IN1C,IN1C,IN1D,IN2,IN2A,IN2A,IN2B,IN2B,IN2C,IN2C,IN2D
IN3,IN3A,IN3B,IN3C,IN4,NC,NC,NC,NC,OUT,OUT,OUT1,OUT2,OUT3,OUT4,OUTA,OUTA,
OUTA,OUTA,OUTB,OUTB,OUTB,OUTB,OUTC,OUTC,OUTD,OX1,OX2,OX3,Q'S,Q1,Q2,Q3,Q4,Q5,
Q6,Q7,Q8,QS,RESET,STROBE,THRESHOLD,TRIG,V2,VC,VDD,VDD,VDD,VDD,VDD,VGGOUT,VOUT
VREF,VSS,VSS,VSS,VSS,
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ANSWER TO BINARY CHOP PUZZLE 5

FLOG LETOH OVARB ATLED MROFINU YAR-X OLIK EKIM EILRAHC ULUZ EEKNAY
AHPLA, APAP REBMEVON TEILUJ AIDNI ARREIS ROTCIV AMIL, OHCE OEMOR
TORTXOF YEKSIHW ORCIM, ILLIM ITNEC ICED, ACED OTCEH OLIK AGEM AGIG
ARET .CEBEUQ RACSO OGNAT OTTA OTMEF ACIP ONAN. SEXIFERP TINU .I.S
TEBAHPLA CITENOHP – BACKWARDS.
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I asked our artist to draw a picture representing a brain teaser, but he must have misheard me! Ed

TEACHER LOCKER

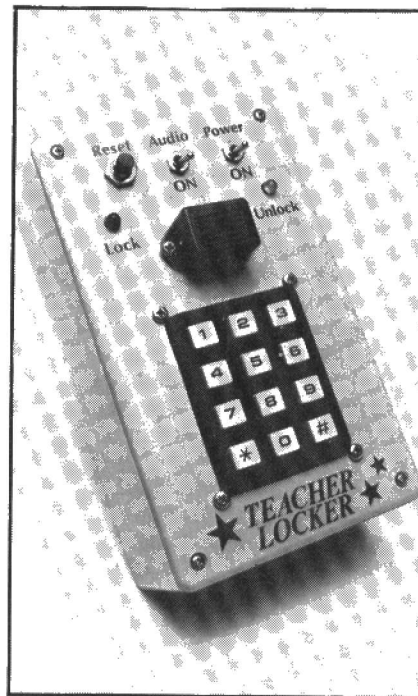## BY TIM PIKE

Even a simple design can give security

The second of a series of articles aimed at giving Secondary School pupils ideas for GCSE projects in Electronics.

FOR the second article in this series I have chosen to look at a range of designs for a simple electronic combination lock. The principle of all such circuits is to combine a number of input switches so that only on particular combination of inputs will activate the final switching device.

In a real security lock, the final transducer would be a solenoid lock or bolt, but in order to keep costs down, the circuits given here end with a simple mains relay. This is activated by a single transistor switch in order to protect the outputs of the logic devices which form the combinational part of the circuit. In block diagram form, all solutions will have common elements. (Fig.1).

TRIPLE AND GATE

One simple implementation of this idea is shown in Fig.2. The AND gate requires that all three inputs are held at logic 1 if the output is to be high. Only when the output of the gate is high will the transistor turn on and hence operate the relay. All other combinations of inputs to the gate produce a logic 0 output (i.e. 'low' level) and hence do *not* turn on the transistor.

The 4k7 resistors connected to the inputs of the gate are known as 'pull down' resistors. They ensure that the

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inputs will be held at or near to 0V unless a switch is pressed.

It is clear that the function of the logic gate is central to the operation of this circuit. One way of improving the sophistication of the lock circuit (and therefore one way of making it more secure) is to change the logic function to one that is more complex. This requires a reasonable knowledge of how logic works, how it is represented and how to design around it. So what are the basic principles of logic?

BINARY LOGIC

At the heart of all work in logic is the assumption that we are dealing with a simple world in which inputs and outputs are either on or off. There are only these two possible states. This suits some devices very well indeed. For example, a simple switch is either on or off. There are no "in between" states. Although a lamp can be thought of as being in many different states, according to its brightness, it is convenient if we allow the lamp only two states as well. The same argument applies to transistors and all the other devices which we might use. By restricting our analysis to accept only one of two states we are defining an electrical system which can be represented perfectly by binary numbers.

The binary number system uses only the two digits 0 and 1. In the positive logic convention, binary 0 is used to represent the low logic level, the off state and therefore an electrical voltage close to zero volts. In the same way, binary 1 is used to represent the high logic level,
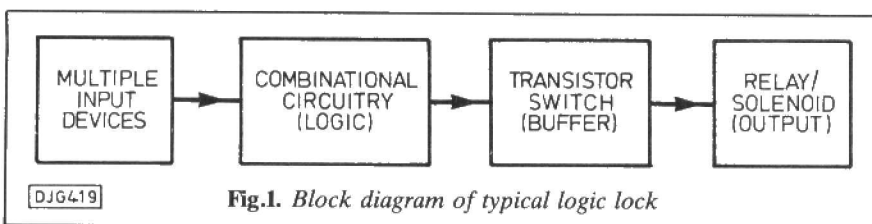

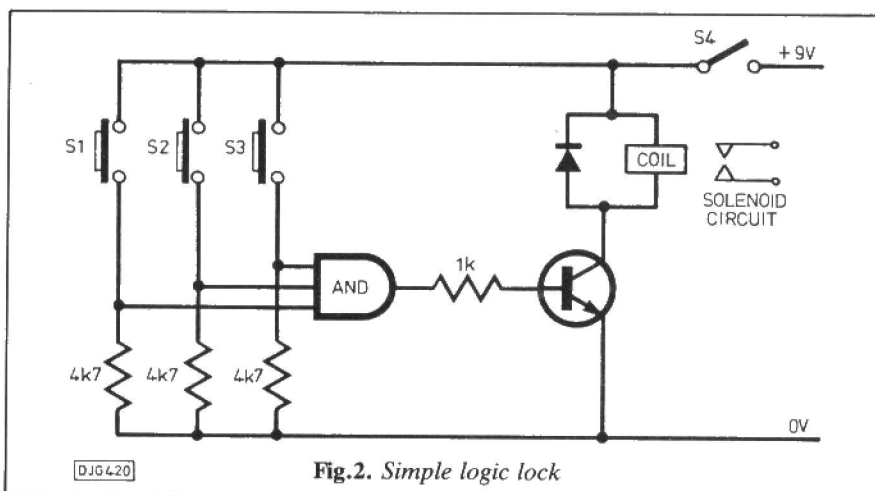**Fig.1.** *Block diagram of typical logic lock*

Fig.2. *Simple logic lock*

the on state and a voltage significantly greater than zero volts, (e.g. +5V or +9V). In general the logic 0 level is held to be 0V and the logic 1 is taken to be the positive supply voltage.

It is very important in logic circuits that all voltages are either close to the logic 0 level or close to the logic 1 level. A voltage halfway between the two would not be clearly one or the other and could therefore lead to a breakdown of the system.

LOGICAL OPERATIONS

In arithmetic, there are the four basic operations, add, subtract, multiply and divide. All arithmetic functions are combinations of these four operations. In order to be able to write down complex operations in a short-hand form, symbols are used to represent the operations.

ADD	+
SUBTRACT	−
MULTIPLY	×
DIVIDE	÷ (or/).

In a similar way there are three basic logical operations. These are AND, OR and INVERT (or NOT).

Other operations can be formed by combining two or more of these three.

NAND is defined as AND followed by NOT.

NOR is defined as OR followed by NOT.

These basic operations can be defined by looking at their truth tables. A truth table is a chart which gives every combination of the inputs to a logic system and, for each, its outcome. For convenience the combinations of inputs are always written in binary order starting with the combination of zeros. The operations AND and OR require at least two inputs. We will call these A and B. The output is represented by F.

TRUTH TABLE FOR OPERATION 'AND'

A	B	F	
0	0	0	Only when both inputs
0	1	0	(in general *all* inputs) are
1	0	0	at logic 1 does the output
1	1	1	become logic 1.

TRUTH TABLE FOR OPERATION 'OR'

A	B	F	
0	0	0	If any one or more
0	1	1	input(s) is at logic 1 then
1	0	1	the output is at logic 1.
1	1	1	

TRUTH TABLE FOR OPERATION 'NOT' (or 'INVERT')

A	F	
0	0	The output is always the opposite state to the input.

BOOLEAN ALGEBRA

It is convenient to be able to write down logical expressions using symbols instead of words. Boolean algebra enables complex operations to be carried out on logical expressions using symbols just as normal algebra does on arithmetic expressions. All we need to worry about at the moment are the symbols for AND, OR and NOT.

The dot (.) means AND
The plus sign (+) means OR
The bar over a letter means NOT

e.g. A.B.	A AND B
A+B	A OR B
$\bar{A}$	NOT A

CIRCUIT SYMBOLS

Logic functions are made up of combinations of logical operations. Each operation is performed by a logic gate. We shall only be concerned with five types of gate, AND, OR, NAND, NOR and NOT.

Although there are a variety of circuit symbols in use, most designers still work with the system shown in Fig.3.
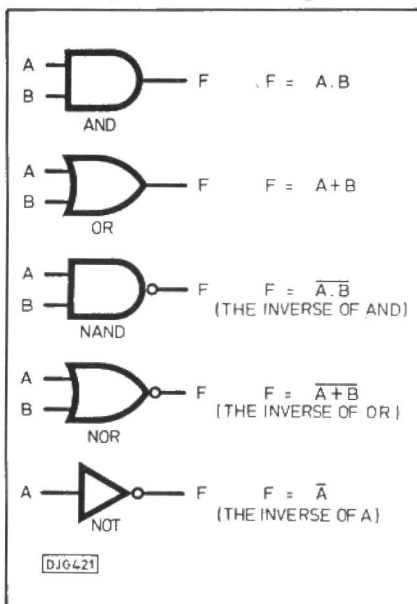

Fig.3. *Basic gates*

It is common for the gates AND, OR, NAND and NOR to have two, three or four inputs. You would choose the type to suit your needs in a particular circuit.

Returning then to the circuit of Fig.2, one AND gate with three inputs is used to 'combine' the effects of the three switches S1, S2 and S3. It would not take a determined burglar long to work out that all three switches must be pressed in order to open the lock. If we are to disguise the operation of the circuit then we need a number of improvements.

MORE SWITCHES

If the number of switches is increased and some of them are 'dummy' switches then the chance of finding the right combination becomes much less.

LATCHING ACTION

With the circuit of Fig.2 as it stands, you would have to keep pressing the switches to keep the lock open. This is obviously not very convenient. Latching switches would not be a good idea because this would leave the lock open until someone else released all the switches. What we need is to latch the circuit after the switches have been pressed. There are several ways of doing this but the most attractive method for GCSE pupils is to exchange the transistor for a thyristor.

The thyristor is a three terminal device which looks like a power transistor but operates like a controlled diode. In fact it is also known as a silicon controlled rectifier (SCR). (Fig.4).
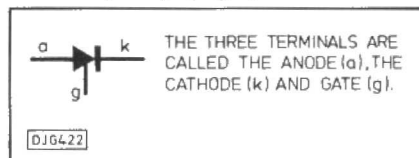

Fig.4. *Symbolic thyristor*

The anode must be positive and the cathode negative if the thyristor is to conduct. Conduction will not occur however, until the gate is also taken slightly positive compared to the cathode. The three terminals work then in much the same way as the collector, emitter and base of an NPN transistor, but there is one important difference. Once conduction has started between anode and cathode, the gate connection can be removed without affecting the current path through the anode and cathode.

Incorporating these two improvements the circuit now becomes that of Fig.5.

Switches S2, S5 and S7 must be pressed together to operate the lock. Switch S9 is included so that the thyristor can be reset after opening the lock. This switch is of the 'push to break' type.

INHIBITORY INPUTS

One weakness of the dummy switches used in Fig.5 is that pressing any of these has no effect and therefore does not prevent the lock from opening. In fact, provided the three switches S2, S5 and S7 are pressed together, any other switches can be pressed as well and the lock will still open. This is a security weakness because pressing all eight switches is one obvious ploy to try. The way to overcome this problem is to build into the logic circuitry one or more inhibitory inputs. These are inputs which must *not* be present if the lock is to open.

In order to keep the logic reasonably simple, suppose that one of the positive inputs is made inhibitory. The logic system can now be represented by Fig.6A.

We need one NOT gate as well as one AND gate. The integrated circuits
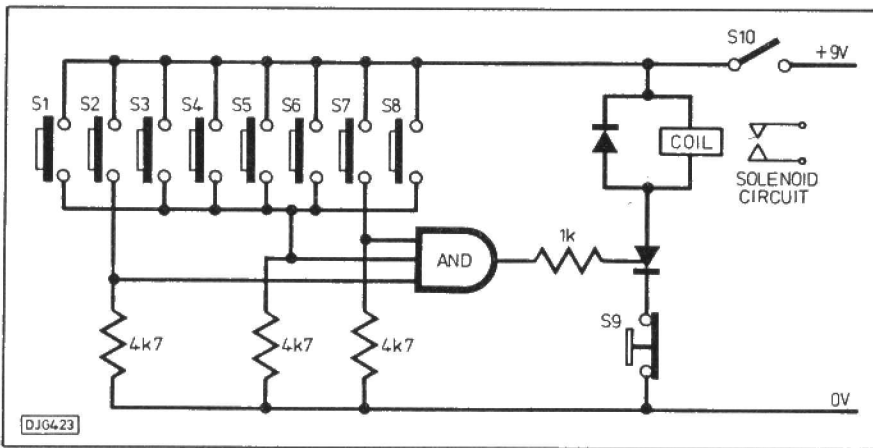
Fig.5. *Improved logic lock*

Fig.7. *Sequential latch*

(CHIPS) which contain the logic gates are almost always of one type only. (There are many other variations but we won't confuse you with that now). So, to produce one AND and one NOT would require two integrated circuits. This is very wasteful since only a small part of each would be used. One chip contains three triple input AND gates, the other chip contains six NOT gates.

The solution to this problem is to convert both types of gate to a common type. The NAND gate is the obvious choice here for two reasons. Firstly because it is so similar to AND and secondly because we need the inverting action in order to produce the NOT gate. A NAND when inverted behaves as an AND gate. A NAND with all its inputs connected together behaves as a NOT gate.

The system is then simply adapted to use only NAND gates as shown in Fig.6B.

gates and thereby ensure a form of sequential behaviour.

In Fig.7 if input 1 is at logic 1 before input 2 then SCR1 will latch on and current will flow through R1. This will take output 1 close to +9V. If then input 2 is taken to logic 1, SCR2 will latch on and output 2 will also be close to +9V. These two high outputs then form the two required inputs to the logic circuitry. If input 2 goes high before input 1, SCR2 cannot conduct because its anode is close to 0V. Output 2 therefore remains at the low level.

By latching the inhibitory input through a single thyristor, if this switch is pressed at any time before or between the two positive inputs the lock will fail to open. A reset switch is needed to unlatch all three thyristors by temporarily removing power from them. The circuit up to the end of the logic arrangement is shown in Fig.8. Switches S2 and S7 must be pressed in this order;
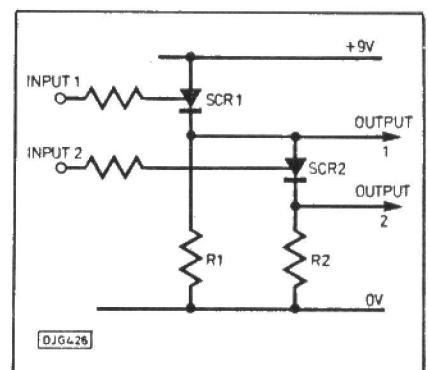
switch S5 must not be pressed if the lock is to open; switches S1, S3, S4, S6 and S8 are 'dummy' switches.

RESETTING

In practice it may be found that direct connections from the cathodes of SCR1 and SCR2 to the inputs of the logic gate might perhaps cause the cathode of the thyristor to remain at a high voltage even when the RESET switch is pressed. The simplest remedy is to connect a single IN4148 diode in between the thyristor cathode and the gate input, in forward conducting style. The loss of another 0.7V in the forward direction does not affect the operation of the gate when the supply voltage in use is 9V. It is worth pointing out that if the circuit were to be re-designed to operate on a 5V supply (for instance because a TTL chip was to be used), then this solution would not allow the proper operation of the gate in the forward direction. The sum of voltage losses across the thyristors and the diode would take the logic 1 level below the threshold for TTL logic 1.
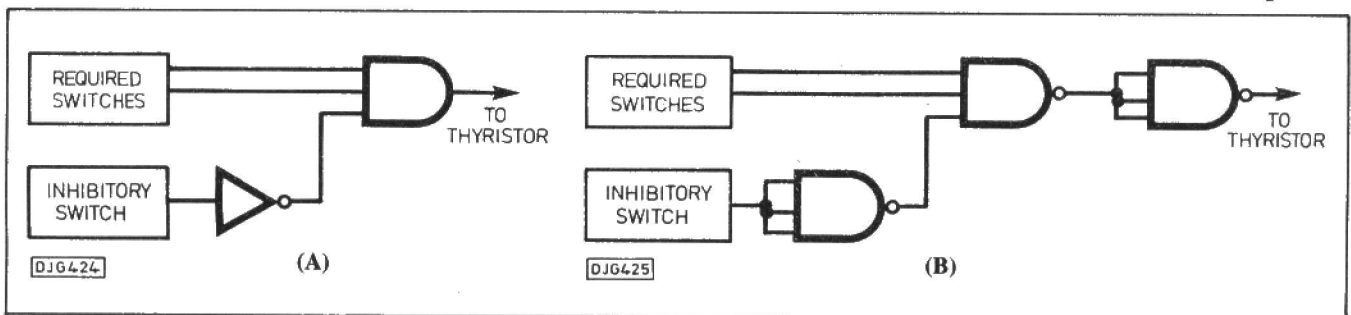
Fig.6. *Two methods for introducing inhibitory switching*

SEQUENTIAL INPUTS

Another improvement to the security of the device is obtained if the required switches have to be pressed in a certain order rather than held down all at once. Entering the numbers in a particular order means that the system must possess some form of memory. Dedicated logic devices which perform exactly this function are readily available from all large component retailers. Our purpose is not served, however, by using one of these devices. If instead we return to the latching circuit obtained by using the thyristor, we can latch the inputs before combining them through the logic
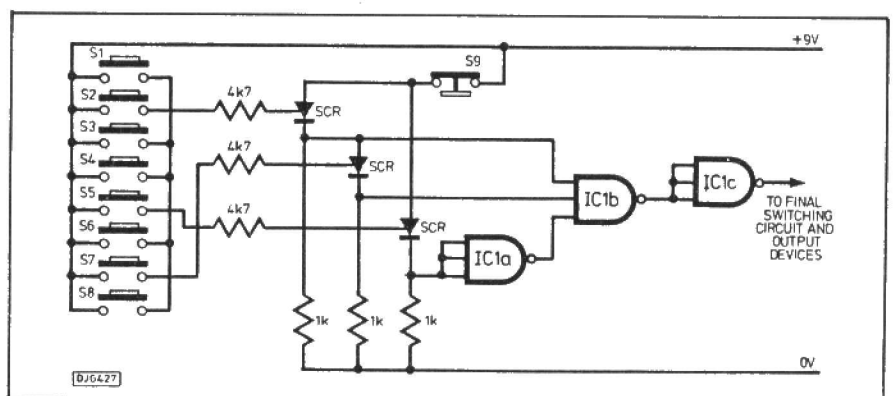
Fig.8. *Coded selective latching*

ADDING AN ALARM

One further possible improvement (and this is certainly optional) is to make more use of the "dummy" inputs. If any of these inputs is used to trigger an audible alarm after a few seconds and at the same time to disable the final relay circuit then the would-be "trial and error" burglar is strongly discouraged.

Triggering an alarm through a simple transistor switching circuit is straightforward. We are using the same principle as that established in the first article in this series, the Teacher Timer Project last month. Using the same signal to prohibit operation of the lock is more sophisticated and should only be considered by the most confident GCSE students. Fig.9 shows the method adopted to sound the alarm.
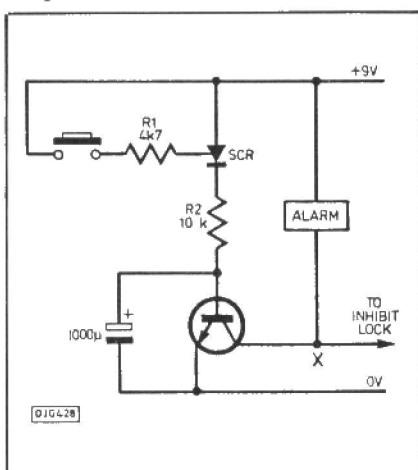

Fig.9. *Alarm switching*

Notice again the use of a thyristor to latch the action of the switch. In practice all the dummy switches from the key pad would be connected in parallel so that any one of them (or more) would have the same effect.

When the thyristor latches, current flows through the anode-cathode path and begins to charge the capacitor. After a short while the transistor turns on and sounds the alarm. It is difficult to produce a delay of more than a second or so unless a very large capacitor is used. The value of resistor R2 in Fig.9 cannot exceed about 10k or else the transistor will not turn on fully when the thyristor latches.

FURTHER PRACTICALITY

There is however one further practical difficulty which would be hard to anticipate but does cause an annoyance. The active audible warning device (AWD) like most devices of this type is 'intermittent' in operation. This means that it is actually switching on and off very fast. Although the transistor will cope with this behaviour, the thyristor which is holding the transistor on is not so happy. Once the gate current has been removed by releasing the switch which caused the alarm to sound, the thyristor needs a fairly stable minimal current in

the anode-cathode path to remain latched on. The intermittent action of the AWD causes feedback of a similarly intermittent signal to the base of the transistor and hence to the thyristor. The result can be that the led is only half on, even though the relay will probably behave correctly. The answer to this problem is to include a steady load R12, in the collector circuit in parallel with the AWD. A 1k resistor works very well indeed.

OPTIONAL EXTRA

It would be perfectly acceptable to leave the design at this level of sophistication. For those of you who would like a further challenge we will now look to see how the operation of the alarm can be made to prevent the operation of the lock.

When the alarm sounds, point X in the circuit of Fig.9 will suddenly drop to around 0V. We need to use this change in the voltage at point X to stop the lock from opening. If you look back to Fig.9 you will recall that we already have one inhibitory input. If we are to limit our design to one requiring only one integrated circuit then we should combine this inhibitory input with all our 'dummy' inhibitory inputs and treat them all as being the same.

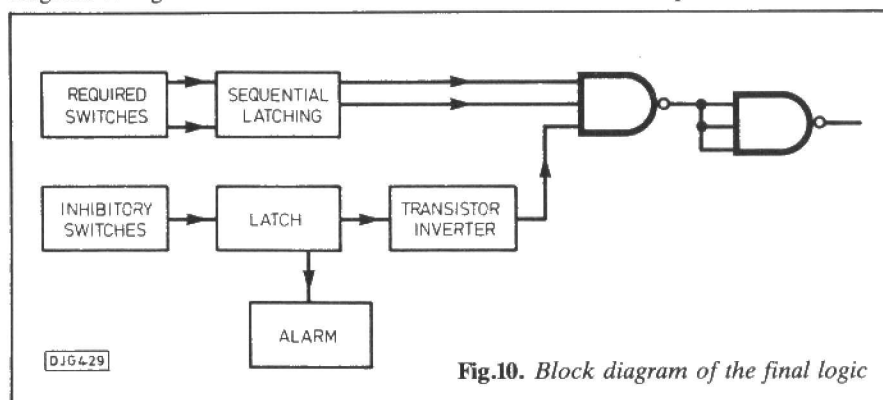The system then looks like the block diagram of Fig.10.

Fig.10. *Block diagram of the final logic*

As is often the case in electronics the addition of another feature actually brings with it a simplification of the overall circuit. We no longer need the thyristor latch for switch S5. Neither do we need the NOT gate to connect this input into the rest of the logic circuit. The transistor switch used to operate the alarm will also act as the necessary inverter.

MONITORING THE OUTPUT

In addition to the green led to indicate the unlock condition, a red led is incorporated to indicate the lock condition. This also serves to monitor the state of the battery or power supply. A second transistor is used to invert the output of the first in order to drive the red led. The complete circuit incorporating all the features discussed is shown in Fig.11.

CHOICE OF COMPONENTS

The logic circuitry requires at least one NAND gate with three inputs. It is most convenient therefore to use one triple three-input package to fulfill both parts of the logic circuit. The choice between CMOS and TTL series is already made if we wish to operate on a +9V supply. TTL will only operate on a very stable +5V supply. Although we could generate this from the +9V battery voltage using a voltage regulator (e.g. 7805) there is no advantage in the extra circuitry and extra cost if CMOS will do just as well. The advantages of TTL over CMOS of faster switching and higher current output are not important in this circuit. The slight disadvantage of CMOS is that it is sensitive to static electricity which simply means that we must be very careful when handling the device. The most important precaution is to earth yourself whilst you are actually handling the Type 4023B CMOS chip. It is also advisable not to wear nylon clothes, and to avoid standing on nylon carpets. Once the chip in the circuit it should come to no harm – at least not from static electricity!

I would strongly recommend the use of a chip socket, which should be soldered into the circuit board at the beginning of construction. The chip itself is not inserted until all other construction is complete and some basic tests have been carried out.

The chosen thyristor is the C106. This type is most commonly used in general practical work in GCSE courses. Although it has provision for a heat sink, no such protection should be needed in this circuit because all currents are limited to 10mA or less.

The switches S1 to S8 could be individual low cost "push to make" switches. Alternatively, an inexpensive miniature data entry key pad with ten or twelve numbered switches may be preferred. Switch S9 is a simple "push to break" switch acting as a reset for the three thyristors. Switch S10 is the on/off switch for the power supply. A miniature SPST toggle is ideal. The relay used in the printed circuit design is a miniature SPDT type rated at 10A at mains voltage.

All other components are readily available standard types.
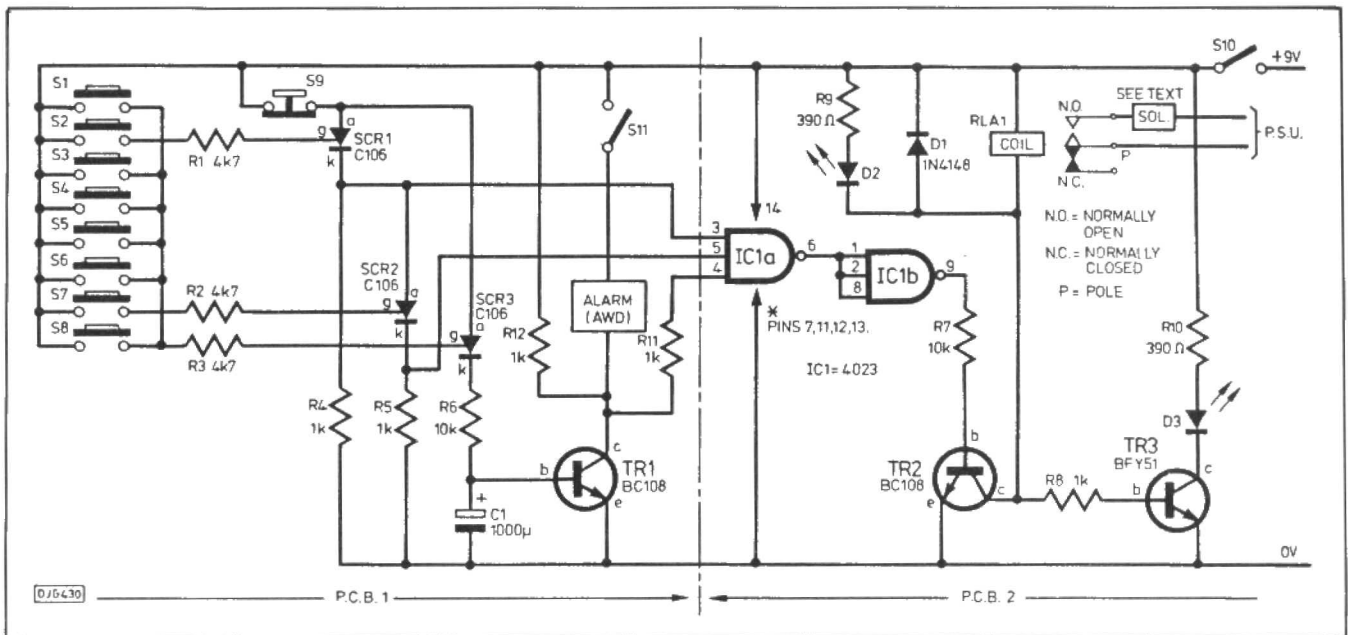
Fig.11. *Complete circuit diagram of the Teacher Locker*

CONSTRUCTION AND TESTING

As the final circuit design is quite complex by GCSE standards, I suggest that the fabrication of the circuit is divided into two parts. Two small printed circuits are easier to work with than one large one. Testing is also much simpler and each board can be thoroughly tested before the whole arrangement is put together.

The two printed circuit designs are given in Fig.12. The most able candidates should be able to work out suitable designs for themselves and this should be encouraged. Alternatively, this circuit can be built quite satisfactorily onto copper stripboard. Make sure that you use the 0.1in matrix to fit the integrated circuit requirements. If the latter method is chosen then it will be necessary to "break" a number of tracks to accommodate the multi-pin devices and to save valuable space on the board. If you choose the printed circuit method and you use the designs given here then you should appreciate that both of these PCB designs have been arranged to fit snugly into an ABS project box. The boards should slide into place vertically between the grooves in opposite sides of the box. The dimensions of the boards are therefore crucial. Each board is shown having dimensions of 84mm by 46mm. A suitable box will have external dimensions of 140mm x 90mm x 55mm.

As well as simplifying the method of fixing the boards into the box, this technique also allows easy interconnection of the boards.

Board "A" needs input connections from the switches and interconnections to the second board consisting of the three logic outputs plus the two power rails. The second board has been designed to be connected to the power source. A 9V battery (PP3 type) is ideal for this purpose.

Ribbon cable makes a very neat job of the interconnections. If you buy the rainbow (i.e. multicoloured ribbon) of the 10 way type you can split off as many or as few ways as you need. It is sometimes possible to buy this cable by the foot (30cm!), and one foot would be plenty for this project.

If you opt for the data entry keypad for your switch panel then again the ribbon cable comes in handy. The keypad plus the two other switches (S9 and S10) need to be mounted on the top surface of the box.

If time permits it would be a good idea to test Board A and check that it works properly before commencing work on the second board. Beyond an initial visual inspection the tests in Table 1 might be carried out on Board A.
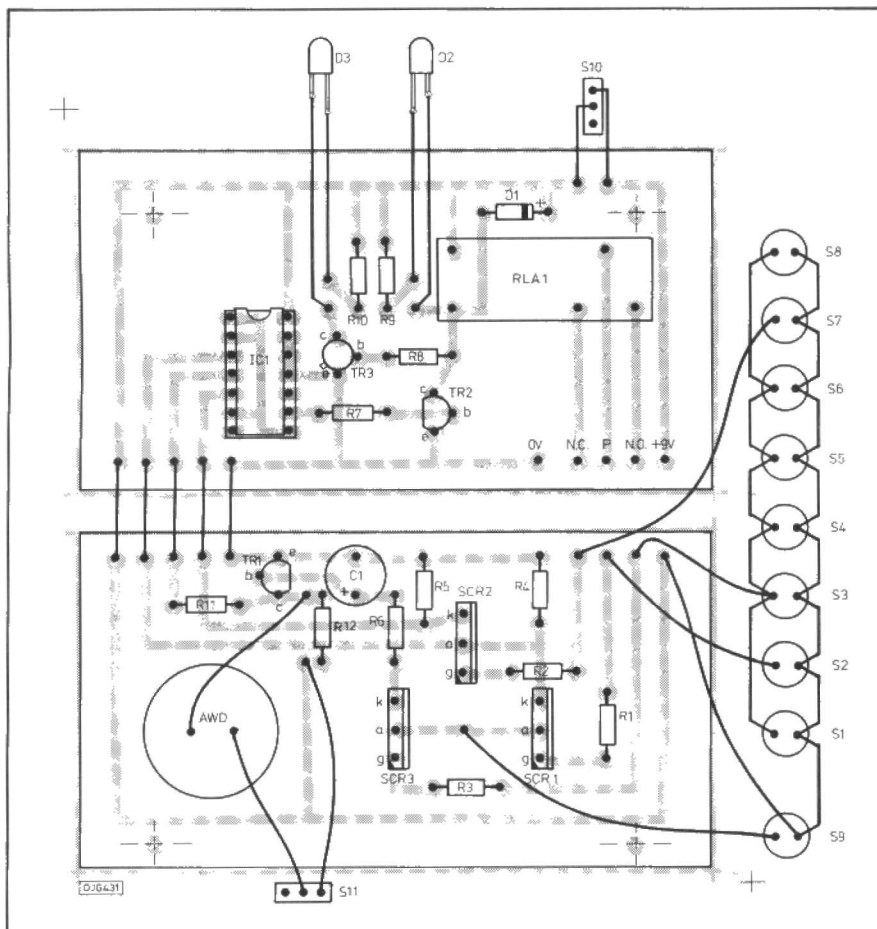
Fig.12. *PCB layout and wiring (using push-make switches)*

TEST POINT	CONDITION	EXPECTED READING
Power rails	Power ON	+9V and 0V.
Switch Outputs S1 – S8	Switches pressed	+9V on each.
Switch Output S9	Switch not pressed	+9V
SCR1 Anode	Switch S9 not pressed	+9V
SCR1 Cathode	Switch S2 not pressed	0V approx.
SCR1 Cathode	Switch S2 pressed	+8.2V approx.
SCR2 Anode	Switch S2 pressed	+8.2V approx.
SCR2 Cathode	As for SCR1	Cathode
SCR2 Cathode	Switch S7 pressed after switch S2	+7.4V approx.
SCR3 Anode	As for SCR1	Anode
SCR3 Cathode	S1 or S3 etc. pressed	+8.2V approx.
TR1 Base	S1 or S3 etc. pressed.	0V rising to 0.7V quickly.
TR1 Collector	S1 or S3 etc. pressed	+9V falling to 0V approx. suddenly

Table 1. Tests on Board A

DIGITAL OR ANALOGUE?

Although in essence this circuit is functioning as a digital device we are using a mixture of analogue and digital components. Serious problems can occur when analogue meets digital or vice versa unless we are very careful with component values.

The three thyristors are being used as latching switches (i.e. digital devices) but of course strictly speaking they are not purely digital. Each thyristor will

TEST POINT	CONDITION	EXPECTED READING
Power rails	Power ON	+9V and 0V.
Inputs and outputs of IC1a and IC1b	Outputs to agree with inputs. (i.e check correct logic function)	All values either < + 2V (logic 0) or > + 7V (logic 1)
Collector Tr2	Base at 0V	+9V approx.
Collector Tr2	Base at 9V	0V approx.
Collector Tr3	Base at 0V	+9V approx.
Collector Tr3	Base at 9V	0V approx.
Relay contacts	Tr2 OFF	N/O contacts open N/C contacts closed
Relay contacts	Tr2 ON	N/O contacts closed N/C contacts open
Diodes D1, D2, D3.	Out of circuit	Check correct function and polarity as necessary

Table 2. Tests for Board B

drop a certain voltage between its anode and its cathode. Thyristor SCR2 is being used 'in cascade' with SCR1; that is to say that the anode of SCR2 is driven from the cathode of SCR1 (they are in series). If the cathode of SCR1 is below 9V when the thyristor is conducting then the cathode of SCR2 will be lower still. These losses are very important since we are connecting the cathodes directly to the input of the logic gate (IC1a). If the losses become too great then the logic pattern will be lost. The actual voltage readings at the cathodes of the first two thyristors are crucial to the correct operation of the gates. When testing it will be important to log accurately what the readings are found to be.

Moving onto the second printed circuit board we might now see the problem in reverse. Given the correct input values, the two logic gates should behave properly and produce the expected outputs either close to +9V or close to 0V.

Since, however, we have chosen to use a CMOS device to produce the logic function, the current which we can draw from the output of IC1b is limited to around 1mA. This current has to drive the base of transistor Tr2 sufficent to saturate the transistor. The saturation current is high because we are running both the green led and the relay coil from this transistor. The led requires around 15mA to light with reasonable brightness. The relay coil requires around 35mA when working on a 9V supply. In total then the transistor must provide at least 50mA (15+35) in the collector circuit. A current gain of at least 50 is therefore required. The choice of transistor for Tr2 is ideally one having a gain of around 100 to ensure that the output of IC1b is not overloaded.

Board B can be tested independently of Board A if the power connections are made and the logic levels are connected directly to the inputs of IC1a. Only when all three inputs are held at or near to 9V should the green led switch on and simultaneously the relay click over. The red led should be on before this condition is satisfied and should then go out as the green led comes on. If you have difficulties with this board then the tests of Table 2 might prove useful.

CONCLUSION

Some students of GCSE may feel that the final circuit as developed in this article is too demanding. It is certainly more complex than candidates would be expected to follow in a theory question set on an examination paper. There are however many simpler alternatives which we have explored along the way. Any of these (even something as simple as Fig.2) would be acceptable at the lower levels of the examination range.

Teachers must play a crucial role in helping each student to be realistic about his or her abilities at the outset of the

project. The chosen circuit should stretch the ability of a student but be attainable by that student. I hope you have some fun with this fascinating topic.

DUAL POWER SUPPLY

BY DAVID SILVESTER

A versatile bench power supply with foldback current limiting

Straight forward to build and adjust, this +/−15V power supply can handle op/amp circuits, but provide enough current for power loads.

THE power supply to be described here has been designed to suit the following conditions:
1) Outputs of +15V, −15V and ground, for safety ground is true earth.
2) Output currents rated to 1.5A for high power applications.
3) Foldback current limiting on both supplies.
4) Cross linked voltage stabilisation, i.e. if one voltage drops due to current limiting the other follows.

Such a supply is clearly capable of providing development capabilities. It is ideal for powering op-amp circuits, which only use very small currents, but since it also has a high current capability, the same +/− 15V supply voltages can drive power loads such as audio amplifiers. Although the circuit itself is capable of higher current output the limiting factors are the output rating of the transformer, the bridge rectifier and the capacitor system providing the unregulated voltage to the control circuit.

THE AC SUPPLY

The circuit of the unregulated AC to DC supply converter is shown in Fig.1. This is a simple reservoir capacitor system with a centre tapped transformer producing two equal outputs of about 35V. A rule of thumb says that with 2000µF per amp of output there will be an AC ripple of 3.5V on the unregulated DC output. For a little better stability, and since they are readily obtainable, 4700µF 63V electrolytic can type capacitors were chosen.
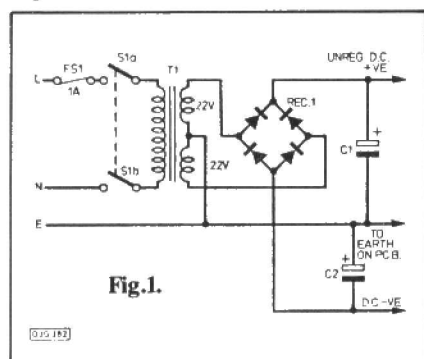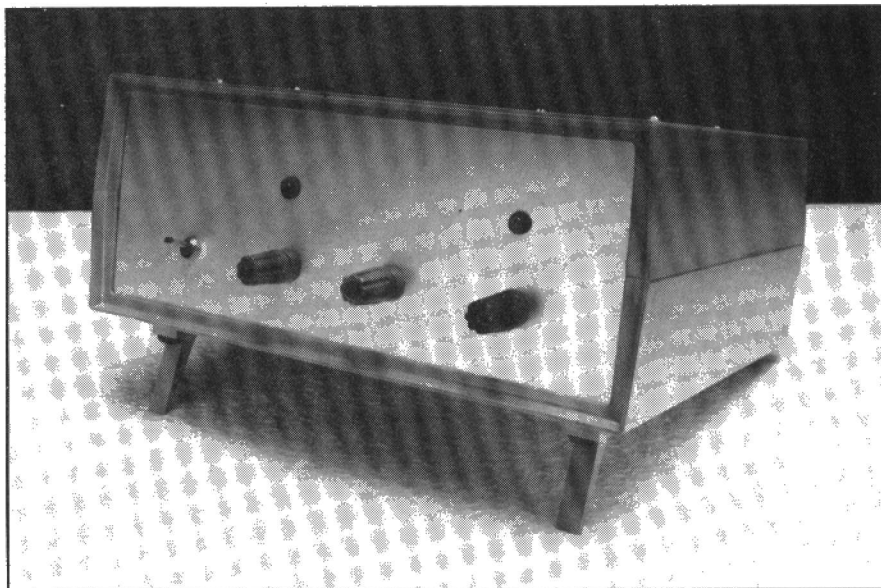

Fig.1.

The bridge rectifier needs to have a working voltage of at least 100V. Under operating conditions double the maximum output, i.e. 70V, will appear across the non-conducting diodes in the bridge at the peak of the AC cycle. The current rating of the bridge is 2A and is adequately in excess of the current limit, which has been set at 1.5A.

The transformer needs to be selected with some care. If too low a rating is chosen the circuit will not operate on current peaks as there will be insufficient voltage differential to allow the semiconductor devices to control correctly. The second factor affecting the choice of transformer is the foldback current limiting system which we shall cover later.

Referring to Fig.3, the current sense resistors of 2.2 ohms give a voltage drop of 3.3V in the current limiting condition. Thus the peak output from the transformer must be greater than or equal to the sum of:—

1) Voltage drop of the current sense resistor — 3.3V
2) Voltage drop of darlington transistor — 1.2V
3) Voltage drop in IC — 5.0V
4) AC drop in reservoir capacitor, min capacity must be used — 3.5V
5) Drop in bridge rectifier, 2 diodes — 1.2V
6) The final output voltage — 15.0V

and this amounts to 29.2V. Since a bridge rectifier circuit of the type shown produces a DC output voltage approximately 1.41 times the nominal AC input, a transformer with a secondary of around 21V AC is required. A transformer will normally deliver its rated voltage when it is supplying its rated current, but under no load conditions the output will be somewhat higher, and for the transformer required here the regulation will be about 15%. A 22V 80W transformer was chosen has a regulation factor of about 15%, giving 25.3V under no load conditions, resulting in an output of 34.5V from the reservoir capacitors.

POSITIVE REGULATOR

The basic circuit of the voltage regulator is shown in Fig.2, and this is needed in two forms to control the two output lines. A stable reference is fed to the non-inverting input of the op amp and a portion of the output is fed to the inverting input. The transistor acts as a pass element. In normal operation the amplifier attempts to hold both input
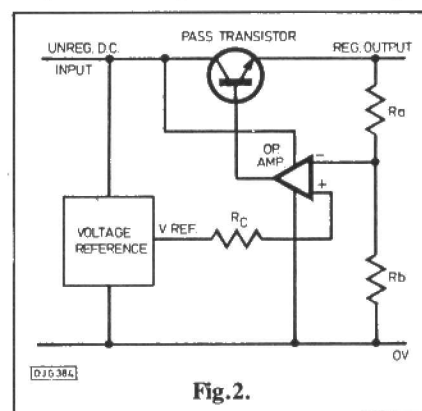

Fig.2.

voltages at the same level, and if $R_a = R_b$ then the output will be twice the reference voltage. R_c is a temperature stablising resistor chosen so that $R_c = R_a R_b / R_a + R_b$ and as far as the op amp is concerned, the reference and output feedback signals seem to come from equal impedances.

Fig.3 shows the full circuit, and in which the positive regulator consists of IC1, R1 to R6, VR1 and Tr1. Ignore C3 at present as this only provides frequency stability, and also ignore the transistor in IC3 which only acts during current limiting of the negative supply rail. R1 is equivalent to R_c in Fig.3. R5, R6 and VR1 provide the feedback, VR1 being added to allow for adjustment of the output voltage when setting up the system. R2, R3 and R4 are concerned with the current limiting.

FOLDBACK CURRENT LIMITING

Foldback limiting is an interesting and rather complicated protection facility so let us consider it in some detail. Fig.4
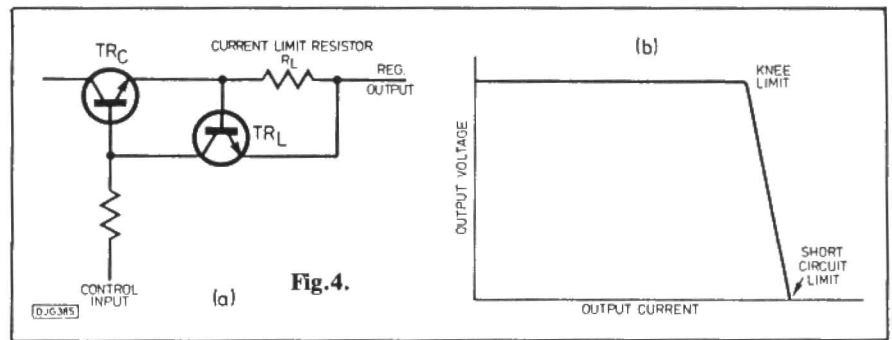
Fig.4.

shows the simple limiter circuit normally used with the 723C, and the output that would be obtained in the limiting condition. If the current through R1 in Fig.4a is below that which will produce a voltage sufficient to turn on Tr1, then the control signal will pass directly to the control transistor Tr_C and the output will be stabilised. If however the current drawn is sufficient to turn on the limiting transistor Tr1, then Tr_C will be robbed of its drive, and the output voltage will fall at a constant current. The knee current and the short circuit current will be

nearly identical under these limiting conditions. The transistor Tr_C will need to drop the power equivalent to the full unregulated DC supply times the short circuit current, and for transistor safety their heat sinks will need to be massive to cope with this overload power. If we can arrange for the current to fall beyond the knee we can save on transistor heat sinks as the power under limiting conditions will fall as the current falls, even though the voltage across the transistor rises. This is precisely the use of foldback current limiting. Fig.5 shows
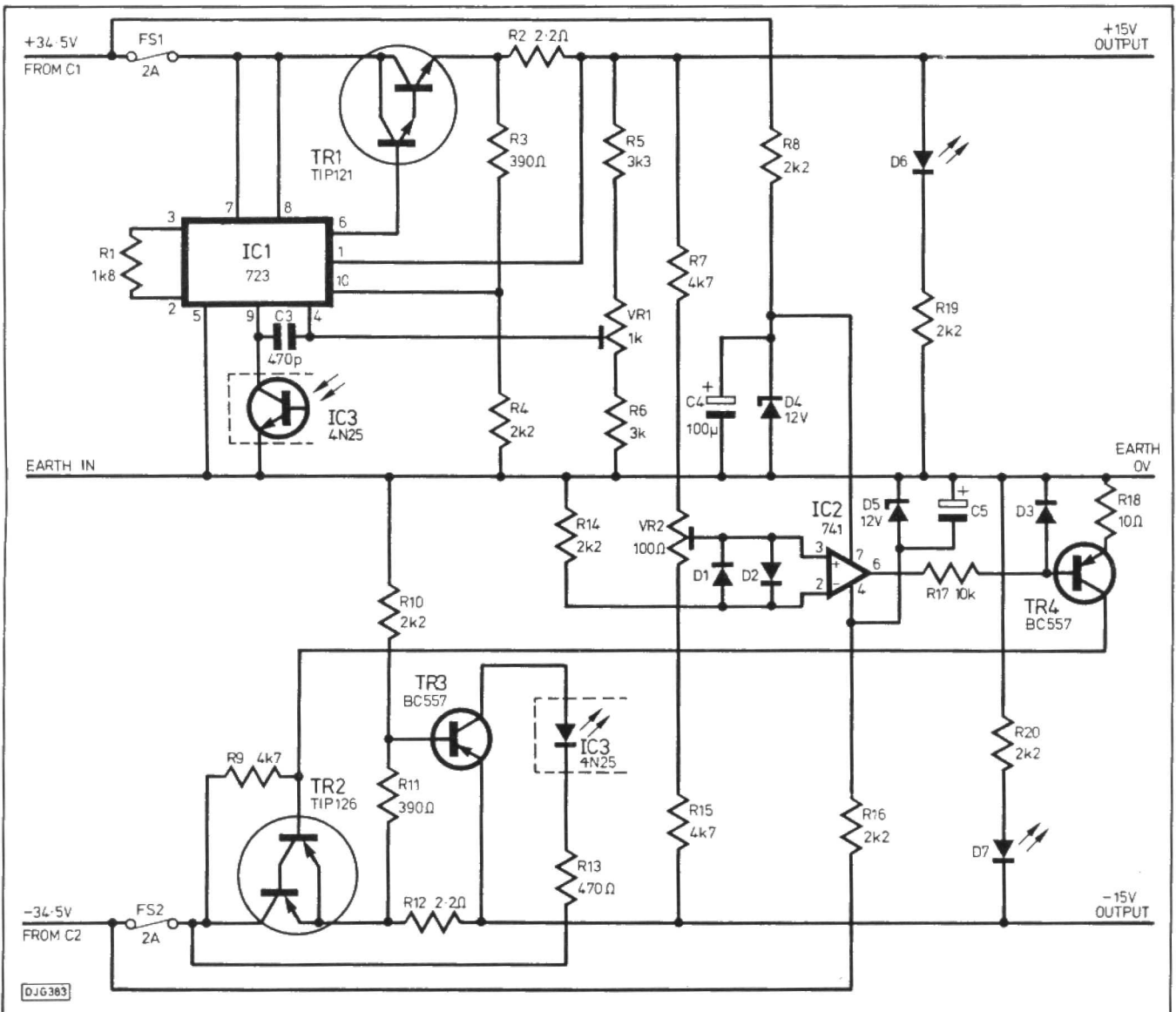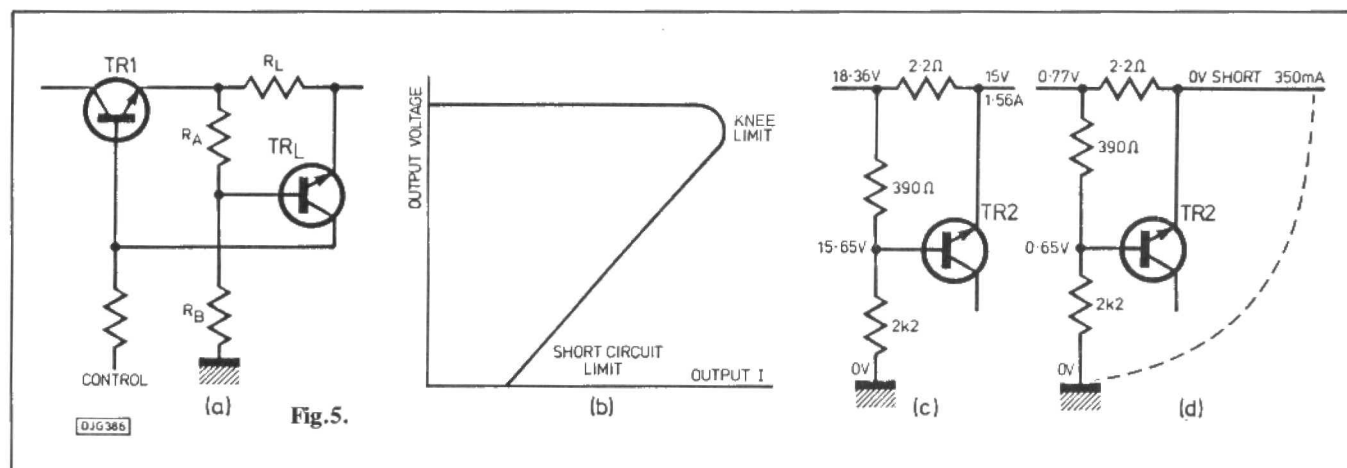

Fig.3. *Circuit diagram of complete power supply*

Fig.5.

the circuit and output diagrams. From Fig.5b it can be seen why this is called foldback limiting. As Fig.5a shows, the circuit is more complicated, as is to be expected with the extra facility that it offers.

Let us look at the circuit itself as shown in abbreviated form in Fig.5a and Fig.5b. At the point when the limiting transistor Tr2 begins to conduct and cut off the drive current, the voltage across its emitter/base junction will be 0.65V. Fig.5c shows the knee condition with an output voltage of 15V and a current of 1.5A. The current sensing resistor of 2.2 ohms is larger in value than that needed for a simple limiting system. Under just-limiting conditions the output from the pass transistor Tr1 is 18.36V, the actual current limit is 1.53A and this voltage is split between the two resistors down to earth. The values are chosen to give 15.65V at the base of the current limiting transistor, and the values calculated are 390 ohms and 2.2k ohms. Under the knee condition the power transistor dissipates 23W.

Now look at the short circuit condition. In this case the output is at zero and the junction of the 390R and 2k2 resistors is at 0.65V. This leads to transistor Tr1 output of 0.77V and a limited current of 350mA. The transistor power dissipation is about 10W; a considerable saving over a power dissipation of 53W for a non-feedback system.

NEGATIVE REGULATOR

Having now established the regulated +15V supply our next consideration is to establish the −15V supply. If we choose a system where we measure the −15V against our established +15V then any fall in the +15V rail will be reflected in the negative supply. Returning to Fig.2, the inputs to IC2 give us a suitable control voltage. One input is tied to earth via R14, which provides impedance matching, as did R1 for IC1. R7, VR2 and R15 control the other input. If the two supplies are exactly 15V then the input voltage at IC2 Pin 3 will be exactly zero. VR2 is included to offset tolerance errors in R7 and R15. The

supply for IC2 is derived from the input supply prior to the fuse FS1. Diodes D1, D2 protect the inputs of IC2 from over voltages, D3 protects Tr4 from positive voltages on its base, and D4 and D5 form

COMPONENTS
RESISTORS

R1	1k8
R2,12	>2R2 watt wire wound (2 off)
R3,11	309R (2 off)
R4,8,10, 14,16	2k2 (5 off)
R5	3k3
R6	3k0
R7,9,15	4k7 (3 off)
R13	47R
R17	10k
R18	10R
R19,R20	2k2 (2 off)

All resistors ¼W 5% unless stated.

CAPACITORS

C1,C2	4700µF 63V electrolytic can type (2 off)
C3	470pF ceramic
C4,C5	100µ16V electrolytic (2 off)

SEMICONDUCTORS

IC1	µA723C
IC2	µA741C (see text)
IC3	4N25 opto-isolator
Tr1	TIP 121
Tr2	TIP 126
Tr3,Tr4	BC557 or any 50V equivalent (2 off)
D1,D2,D3	1N4148 (3 off)
D4,D5	12V 400mW zener (2 off)
D6,D7	LED (2 off)
REC1	100V 2A bridge rectifier

POTENTIOMETERS

VR1	1k 20 turn preset
VR2	100R 20 turn preset

MISCELLANEOUS

Transformer 80W 22V, PCB DPDT mains switch, case, 3 output sockets, 2 PCB mounting fuse holders and 2 amp fuses, panel mounting fuse holder and 1 amp fuse, 2 grommets, heatsink to suit, fixings and stand offs as required.

a zener stabilised supply for IC2.

The rest of the −15V stabilising circuit is very simple. R9 tries to turn on the pass transistor Tr2 whilst Tr4 under the control to IC2 tries to turn it off. Equilibrium is achieved when both supply outputs are balanced and with the two inputs to IC2 equally at zero volts.

IC2 can be practically any op-amp from an ordinary 741 to the latest JFET and MOSFET types providing that the pin configuration is compatible. 741Cs, LF351s and CA3140s have all been tried with identical results.

NEGATIVE CURRENT LIMITING

The current limiting for the negative supply is interesting in that it turns off the positive supply voltage and obviously the negative supply follows it. Like the positive supply, current limiting is of the foldback type. Any current sufficient to turn on Tr3 illuminates the LED in IC3. This is an opto-coupler in which the transistor is connected to IC1. By shorting pin 9 of IC1 to earth the output voltage can be reduced to zero. Now, as the negative output follows the positive output, if the voltage of the positive supply falls due to current limiting in the negative supply rail we obtain true current limiting in the negative rail, and additionally a fall in both supply rails if either rail is subjected to current limiting.

CONSTRUCTION

Construction is extremely simple as most of the circuitry is built on a single sided PCB (Fig.6). The two power transistors are mounted on a heat sink which is fitted to the back of the case. The power resistors need to be mounted on the PCB allowing a substantial gap between the bottom of the resistor and the top of the board as the heat from these could seriously damage the board. The transformer, bridge and reservoir capacitors are fitted directly to the case and hard wired with positive, negative and ground/earth wires passing to the PCB. The ground is connected directly to mains earth, and standard mains wiring safety rules must be observed.

Fig.6. *Printed circuit board layout and connection details*

From the PCB the output goes to the front panel. Output line monitoring is by means of LEDs across each output.

To align the system only two pots need to be set. VR1 is adjusted until the positive output is +15V with respect to ground, and following this VR2 is adjusted to set the negative output to −15V. As the negative supply follows the positive and any error in the positive supply will be reflected in the negative supply, VR1 must be set before VR2.

OUR REGULAR LOOK AT ASTRONOMY

SPACEWATCH

BY DR PATRICK MOORE OBE

The Royal Greenwich Observatory loses Herstmonceux to time share flats. But it is too early to start planning a holiday on another solar system.

PERHAPS the most depressing news this month is that, of all accounts, there is now a serious proposal to sell off Herstmonceux Castle as time sharing flats. There now seems little doubt that the Royal Greenwhich Observatory will move to Cambridge – though Cambridge does not want it, and Sussex does not want to lose it. The thought-processes of bureaucrats do indeed defy all reason. On the credit side, the William Herschel Reflector at La Palma is performing well, and will be in full operation shortly; so too is another British venture, the James Clerk Maxwell Telescope on Mauna Kea in Hawaii, which is designed to study microwave radiations from space.

The supernova in the Large Cloud of Magellan has faded markedly, and the main outburst is definitely over. (In fact, it was over 155,000 years ago, though we have only just observed it!). There is now no doubt that the blue supergiant really was the progenitor star, and this means that some of our cherished theories about the later stages of stellar evolution may have to be modified. There is, of course, a strong possibility that the star had already passed through a red giant stage. Whether it will produce a pulsar remains to be seen; within a few months we should know.

Spectroscopic studies of the amounts of two elements, thorium and neodymium, in various stars have led Professor H. Butcher, of the Kapteyn Astronomical Institute in Holland, to suggest that the age of the universe (in its present form) is less than has been believed; he gives an upper limit of 10,000 million years. However, evidence indicates that some objects known to us are further away than 10,000 million light-years, so that there is a major discrepancy; we must await the results of further research.

Sadly, we must record the deaths of two distinguished astronomers. Professor Bengt Strømgren, of Denmark, has died in Copenhagen at the age of 79. He spent much of his career in America, and was for some years Director of the Yerkes Observatory, near Chicago; he made major contributions to stellar and interstellar research. On 17 July Dr. David Brown died at the early age of 59. Dr. Brown was renowned for his skill in optical working, and was the leader of the team at Grubb Parsons which was responsible for a whole succession of telescopes, including the 165-inch William Herschel mirror which has now been brought into use at La Palma. His early death is a sad loss to astronomy as well as to his many friends all over the world.

EXTRA-SOLAR PLANETS?

The search for planets of other stars is one of the most fascinating branches of research in modern astronomy. There seems little doubt that they exist – but providing positive proof is quite another matter. No telescope yet built is capable of showing even a large planet attending a relatively nearby star. However, P. van

The Sky This Month

BOTH the giant planets, Jupiter and Saturn, are on view this month. Saturn lies in Ophiuchus, the Serpent-Bearer – which is not officially recognized as a Zodiacal constellation, but which does intrude into the Zodiac between Scorpius and Sagittarius. Saturn is half a magnitude fainter than it was at opposition in June, but it is still easy to recognise, and even in a small telescope it is a superb sight, because the ring-system is wide open. Look also for the main satellite, Titan, which is one of the most fascinating worlds in the Solar System; it has a dense atmosphere, made up largely of nitrogen, and we can only speculate as to the conditions below Titan's clouds. There may be a methane or ethane ocean!

Jupiter, in Pisces (the Fishes) is approaching opposition, and is a brilliant object for the greater part of the night; its magnitude is −2.8 – fully a magnitude brigher than Sirius, the most brilliant of stars. A modest telescope will show Jupiter's cloud belts, and also its four main satellites, the Galileans. This is also a good time to see whether any of the galilean satellites can be glimpsed with binoculars. Three of them (Io, Ganymede and Callisto) are larger than our Moon, and the other (Europa) not much smaller. The Voyager probes have shown that they are not like each other; Ganymede and Callisto are icy and cratered, Europa icy and smooth, and Io red and volcanic. However, from Earth, they appear only as tiny disks.

Of the other planets, Mercury is theoretically an evening object, but is so far south of the celestial equator that it is not likely to be a naked-eye object from Britain. Venus and Mars are on the far side of the Sun, and to all intents and purposes are out of view altogether.

The Moon is full on 7 September, and new on the 23rd. On the 23rd there will be an annular eclipse of the Sun – when the lining up is more or less exact, but the Moon appears smaller than the Sun in the sky, so that a ring of sunlight is left showing round the dark lunar disk. Unfortunately the eclipse will not be seen from Europe; you will have to go to Asia or Australasia – and it must be admitted that an annular eclipse if far less spectacular than a total eclipse, since the corona and prominences do not appear.

There are no important meteor showers this month, and no naked-eye comets are expected – though, of course, one never knows!

de Kamp and his colleagues at the Sproule Observatory in the United States have claimed that they have detected planets by astrometric methods – the perturbations caused in the proper motions of some stars, notably Barnard's Star, which is a faint red dwarf only 6 light-years from us, and therefore the nearest star to the Solar Systems apart from those of the Alpha Centauri group. Also, the IRAS satellite detected infra-red material associated with several stars, including Vega, Fomalhaut and Beta Pictoris, which could be interpreted as planet-forming. But van de Kamp's results have been challenged, and we have no proof at all that the infra-red excesses of Vega and the other IRAS targets indicate the presence of actual planets.

Now, three Canadian astronomers – Bruce Campbell of the Dominion Astrophysical Observatory in British Columbia, and Gordon Walker and Stephenson Yang of the University in Vancouver – claim that they have found indications of planetary companions to seven stars, most notably Epsilon Eridani and Gamma Cephei. What they have done is to measure the velocities at which these stars are approaching us, and to detect variations in these velocities which may be interpreted as due to perturbations by planetary companions. Epsilon Eridani has long been one of our favourite targets; along with Tau Ceti it is the nearest star which is reasonably like our Sun, and is single – though it is somewhat smaller and cooler, with a spectrum of type K. It was one of the targets for the famous project Ozma of more than a quarter of a century ago, when radio astronomers at Green Bank, Western Virginia, set out to see whether any rhythmical signals could be picked up from the system, though, not surprisingly, the results were negative.

Gamma Cephei, or Alrai, is different; its distance is given as 52 light years, and it is about 9 times more luminous than the Sun. All the same, it is not an unreasonable candidate as a centre for a planetary system.

How reliable are these results – and what do they really mean? If they do in fact indicate the presence of planets, then these planets must be much larger and more massive than the Earth, and probably more massive than Jupiter. It is fair to say that while the results are interesting, they are far from conclusive, and it would be most unwise to make any grandiose claims. We will – we hope – learn more with the launching of the Hubble Telescope, the 94-inch reflector which is scheduled to be put into a path round the Earth above the top of our inconvenient atmosphere; but just when this will happen must depend upon how quickly the American space programme can recover from the *Challenger* disaster.

PE

COLLECTOR OMITTER BASE

Electronic technology abounds on the London Underground, not least on ticket control methods. In particular, automatic ticket checking gates are now widely used at many station exits and entrances. It is no doubt expected that these will help cut down on ticket fraud and fare dodging.

However, a dodgy interface link still remains, as I recently witnessed. At a station barely a full stop away from the Ed Office, ticket collectors are still used, but occasionally are absent. Some honest passengers coming out of the station then leave their used tickets, magnetic or otherwise, on the counter of the collector's desk.

This honesty though, can lead to greater fraud. Coming out past the vacant counter the other morning, two people pushed passed me on their way in, grabbed a handful off the ticket pile, and disappeared down the escalator. Quite likely they and others do this whenever possible, enjoying wide spread free travel.

It seems that London Underground may have an emitter-collector junction problem – a semi-automated system that is far from foolproof, and all too user-friendly.   **Ed.**

SINGLE PORT EPROM PROGRAMMER

BY MALCOLM HARVEY

Fast flexible and useful – and possibly unique

A versatile programmer, designed for the fast, low-power TMS 2532A EPROM and its compatibles. The PET Basic is readily adaptable for computers with similar data ports.

OF the various computers to which I have access, I confess to a particular liking for a machine that is now over seven years old – the Commodore 3032. It has proved itself to be a good hardworking computer and, as a quick calculation, has probably processed in excess of 100 million million bytes. However, by current standards, its 32K memory is tiny and leaves little room for some operations, though it is remarkable how such restrictions discipline programming techniques.

So, this Christmas, feeling too overfed to be energetic, I decided that it was time that some of my resident code subroutines could probably be better placed by putting them into ROM, releasing 4K of RAM. (As I write this, I am conscious that some readers may well have machines with 512K, and be much amused at the thought of only 4K extra.) These routines include such essential operations as Sort, Search, DOS, Repeat Key and Date Validity – these ought to be standard facilities on all micros, especially Sort which in machine code can save hours.

OFF THE MENU

Anyway, having decided to move 4K from RAM to ROM, I started looking through back issues of various electronics magazines for a simple EPROM programmer. Whilst I do not claim to have looked through all, I was surprised to find that none really offered what I wanted. Some were highly sophisticted units allowing programming of every conceivable EPROM type, shape and size; others were already built in to dedicated systems; some were seen in which multiple ports were required to send address data, byte data, and handshake signals direct from a computer; and still more that would do the job for me if I didn't mind entering 4K of data by hand as separate bits (imagine having entered 4K x 8 bits, only to make a mistake on the last one and having to erase and start again).
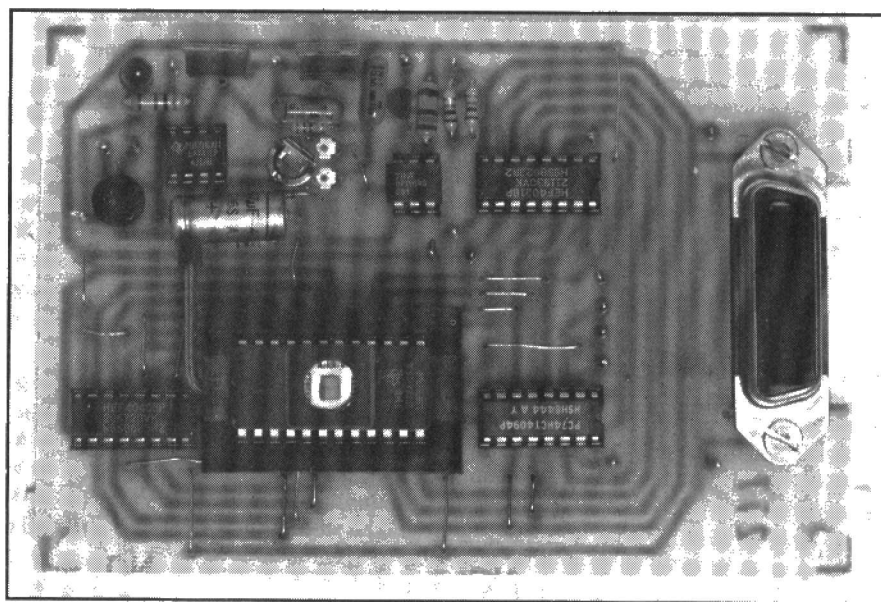
It eventually became apparent that what I wanted, a computer controlled programmer using a single 8-bit parallel port, had probably not been published. (Possibly I shall now be inundated with letters telling me which magazines I overlooked). Consequently, it seemed that if I wanted this particular method, then probably other people did too, and so on the Sixth Day of Christmas I avoided the final shreds of the turkey, and did a bit of track laying. The resulting PCB is herewith now presented!

BASIC ESSENTIALS

Before setting to the PCB itself though, it is preferable to discuss the basic necessities a bit. The circuit has been designed to program a 4096 byte EPROM, specifically the TMS2532A, though it is suitable for other EPROMS, as will be discussed later. EPROM, is short of course, for Erasable Programmable Read-Only Memory. The erasing can only be done by exposing the device to ultraviolet light, but the programming is done electronically. The basic requirements are that the byte of data to be programmed is presented on one set of pins, and the address at which it is to be stored is presented at another set. Then a programming pulse is sent to another pin, and causes the data to be stored at the address specified.

The data byte is 8 bits wide, and since the total number of addresses available is 4096, the address port is 12 bits wide (2^{12} = 4096). Including control of the programming pulse, 21 pins have to be under simultaneous control. In order to control 21 lines from a computer output port having only 8 data bits and two handshake lines, there are two options open. One is to send three separate blocks of data, storing them as a registered set, and then sending the programming pulse. The other, and that used here, is to translate the parallel data into serial form, to use a clocked counter to control storage addresses, and then send the programming pulse. This may appear to require only 3 lines to control the full cycle, but in practise, the circuit actually uses all 8 data lines, plus a handshake line.

The sequence of control line levels can be read in the accompanying Basic section of the program listing. In essence though, the sequence is as follows. First reset the counter. Send eight separate data bits to a serial to parallel converter, clocking each bit through the converter as it arrives. After the eighth bit, open the converter so that the stored parallel byte is presented to the EPROM. Then send the high level programming pulse, close the converter, and send a clocking pulse to the counter, stepping it on by one place.

An additional read back facility has been provided that converts the EPROM output into a serial form for feeding back to the computer on another line. This needs the 8-bit byte to be clocked through using a register storage pulse, and a series of eight stepping pulses. Thus nine control lines are needed. Here the serial to parallel converter is triggered by a handshake line, and the eight data lines carry the remaining signals.

EPROM TMS2532A

In order for the EPROM to store the data in a permanent form (until erased by UV light), a programming pulse well in excess of the 5V normal power line level has to be applied to the relevant pin. Known as the Vpp level, this can vary between EPROMS in terms of the pin to which it is applied, and the minimum voltage level that will allow storage. Usually EPROMs require the Vpp level to be at 25V, and for the pulse to last for at least 50 milliseconds. The TMS2532A has been designed to operate at a lower Vpp of 21V, which, though still not within the control of many semiconductor switches, can be readily controlled by an opto-isolator device.

The TMS2532A also needs a minimum pulse duration of only 10 milliseconds and this improvement has the obvious advantage of speeding up the total programming time, cutting it from several minutes, to around 45 seconds. It is also interesting to note from the manufacturer's data sheet, that if simultaneous programming and monitoring is performed, the controlling software or hardware program can determine the precise moment at which the EPROM accepts the required data, so potentially allowing Vpp pulse widths to be automatically tailored to absolute minimum durations. However, this unit and its controlling program have been designed for most post-program checking, and so uses a consistent Vpp duration. This though can be varied from the computer prior to programming so that any pulse length can be set. Consequently the unit is equally suited to normal EPROMs requiring the longer 50 millisecond pulses. Incidentally, the TMS2532A will also readily accept the longer pulse.

FULL DESCRIPTION

Let's run through the precise functions and operations. IC2 is a divide by 4096 counter, having 12 output lines that together determine the EPROM address at which the required program data is to be stored. It is initially reset to zero by a high going level from computer line DA2. Then, during the programming sequence, the address is clocked up by one place each time line DA6 transitions from high to low. It is not possible to select random EPROM addresses, and they will occur in strict numerical sequence from 0 to 4095. It is however possible for the computer program to step the counter through to a later address than zero before actually sending data to the EPROM, consequently sectional programming is possible, with the obvious advantage of allowing a partially programmed EPROM to have unused areas filled with fresh data.
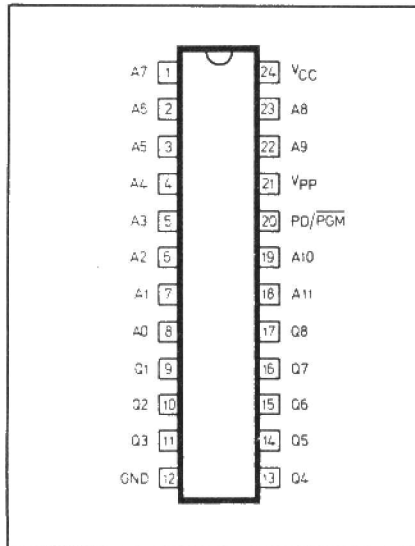

Fig.1. *TMS2532A pin connections*

SERIAL TO PARALLEL

IC1 is a tri-state serial to parallel converter. This means that its output can be held in a high impedance state until the chip is instructed to pass its stored data to them. The data is fed bit by bit along line DA0, and as each bit is sent, a clock pulse from the line ATN causes it to be stored in internal registers. On receipt of each positive going clock pulse, each of the eight internal registers passes its data to the next register in series. After eight clock pulses, the relevant levels of an 8-bit data byte are held in their separate registers. Since the outputs are in a high impedance state they have no affect upon the EPROM until they are enabled by data line DA1 going high.

VPP CONTROL

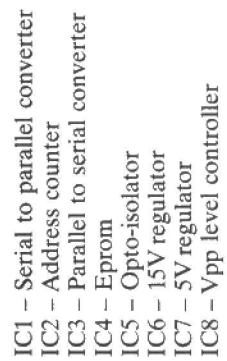Once the register outputs are open, the computer line DA5 is sent high, so causing TR1 to conduct. Its collector is in series with the current limiting resistor R3 and a LED inside IC5. The LED turns on and illuminates an optically sensitive transistor also within IC5. In response, the internal transistor conducts the high voltage level from the power supply through to the EPROM Vpp pin. After a preset duration, the computer takes DA5 down again, so removing the Vpp level from the EPROM. By the end of this pulse, the data byte from IC1 will have been stored by the EPROM at the address dictated by the counter IC2. In the absence of the high level Vpp, a lower level of around 5V must be maintained on the EPROM control pin. This comes from the 5V line via D2, with R5 supplementing the normal control and acting as a leakage path following the end of the pulse.

PARALLEL TO SERIAL

Once the required number of data bytes has been programmed into the EPROM, the computer program commences checking that they have been correctly stored. During this sequence the Vpp level is held low by line DA5 and the serial to parallel converter IC1 is held with its outputs in a high impedance state. Counter IC2 is reset to zero, and then stepped if necessary to the required starting address. The data stored at the set address is now available on the bi-directional lines that have previously been receiving information from IC1. Since IC1 is closed, it has no affect on these levels. To these lines is connected the parallel to serial converter IC3. Upon receipt of a high going pulse along line DA4, the internal registers of IC3 accept the data byte, and store it when DA4 goes low again.

Each time a positive going clock pulse from DA3 is received, the internal registers pass their data along in series from one to the next. The output of the eighth register is available at pin 3 via DA7, and at each step DA7 is read by the computer and the data temporarily stored in memory. At the end of eight steps, the memorised answer is compared with the number held in the memory area from which the data originated. If the match is successful, IC2 is stepped on by one place, and the sequence repeated. In the unlikely event of a mismatch, which would indicate incorrect operation of the EPROM programming, the computer aborts its routine and signals its dissatisfaction on the screen. If all EPROM and Memory data bytes match, the programming has been satisfactorily completed.

Since this checking sequence can be stepped through rapidly, the rate is limited only by the speed at which the computer can process the controlling. With the machine code program listed,

Fig. 2. *Full circuit diagram of the Single Port Eprom Programmer, including power supply.*

IC1 – Serial to parallel converter
IC2 – Address counter
IC3 – Parallel to serial converter
IC4 – Eprom
IC5 – Opto-isolator
IC6 – 15V regulator
IC7 – 5V regulator
IC8 – Vpp level controller

and a computer clock speed of 1MHz, it takes less than 2 seconds, compared with around 45 seconds for the storage operation, as discussed above.

POWER SUPPLY

The unit can be supplied either from the optional mains to d.c. converter shown, consisting of T1 and the bridge rectifier, or it can be supplied by an existing d.c. unit. In either case, the d.c. level, which should be at least 2V above the final output voltage required, passed through IC6 and is partially fed back to it via IC8. VR1 controls the feedback and thus the output voltage, and should be set for the Vpp level required by the EPROM type used. A monitoring pin is incuded on the PCB to enable a voltmeter to be connected. VR1 offers a good margin of control and should be set as close as possible to the specified level, within less than half a volt either side.
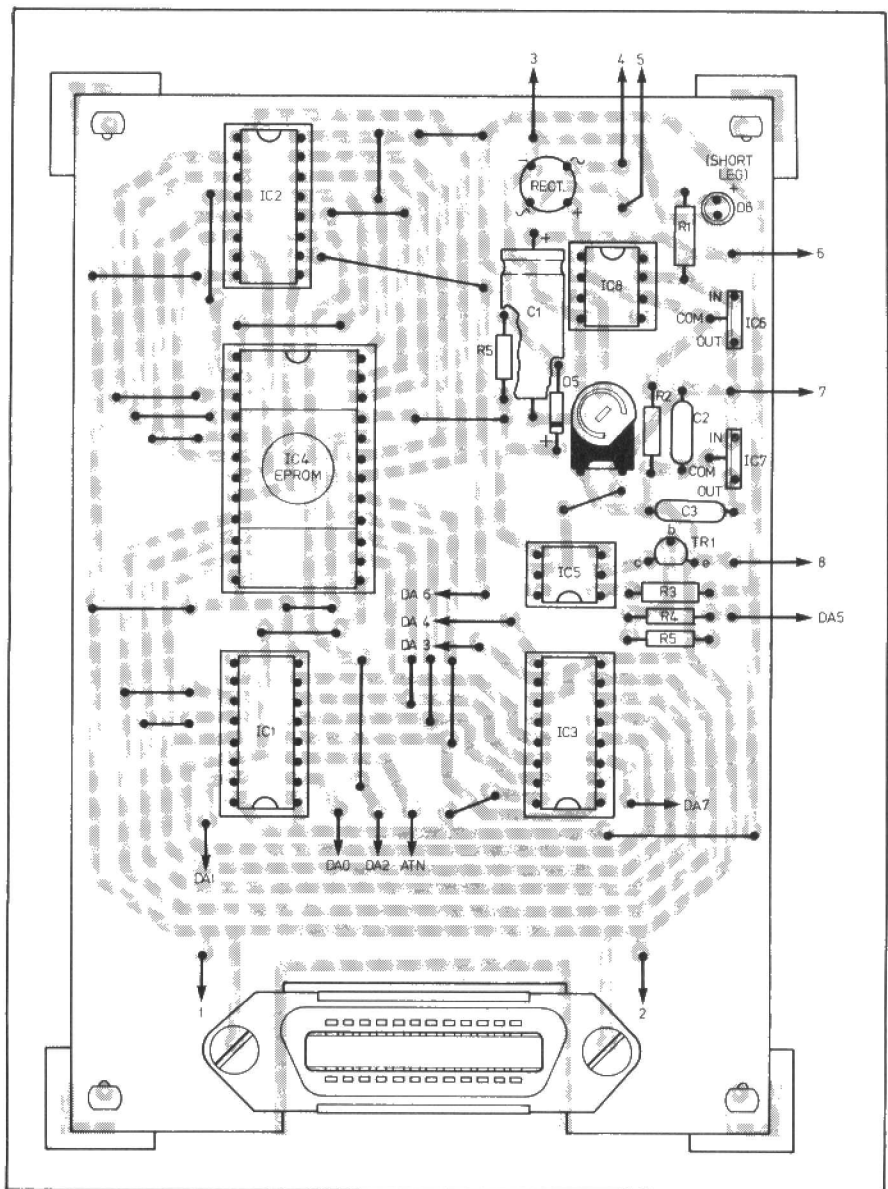
IC7 regulates the Vpp line down to the 5V level required by the rest of the circuit. Since even in its quiescent state the EPROM may well draw at least 50mA, IC7 will probably set rather warm, but still remain within its thermal and current limitations, even if the circuit remains switched on for longer than the required programming and checking time. If you do think about connecting a heat sink to it (I have felt no need to), it can be bolted to the side of any metal case used. In no way should IC6 be bolted to the case, or connected to ground, or to IC7.

If the optional mains supply is used, the transformer secondary winding should be selected to suit the final current and voltage required. The rectified d.c. voltage for a given secondary will be approximately 1.41 times the nominal a.c. voltage. Due to load and tolerance factors, a high level may usually be experienced, consequently an 18V secondary with a current rating of about 100mA will probably be satisfactory. If an 18V transformer is not available a 0–9V 0–9V one could be used connecting the windings as shown in Fig.4, or a 9V-0-9V could be used, ignoring the central tapping.

Note that the power supply must not be switched on with an EPROM in the socket until the computer program tells you to. Failure to observe this could cause spontaneous programming of random EPROM addresses.

PRINTED CIRCUIT BOARD

Provision has been made on the PCB for the rectifier and C1 to be included if the mains PSU is used. In this instance it is imperative that the transformer and all mains connections are kept in an enclosed box, and that the PCB should not be in the same box, unless you make absolutely sure that when inserting EPROMS, there is no chance of

touching mains connections.

Wire links on the PCB can be made from single strands of connecting wire. The computer lead socket may be mounted directly to the PCB, cutting out a suitably shaped slot in the area provided. In my unit, a standard 24-way IDC socket was used. DIL sockets should be used for all ICs, and if a lot of EPROMs are to be programmed, it is suggested that the EPROM socket should be one of the Zero Insertion Force type (ZIF socket). These have a lever at one end that opens up the socket holes allowing easy insertion of the EPROM. However, since they are expensive, I suggest that an ordinary 24-pin DIL socket is soldered into the PCB, and then the ZIF socket can be inserted into that, allowing it to be removed if required for another circuit, so minimising overall expense.

COMPUTER PROGRAM

The program has been written in PET Basic, but information is included in the

program listing enabling it to be used with the Commodore C64 or the BBC. Data port connections for all three computers are shown in Fig. 4. Those of you who are knowledgeable in machine code will see that by substituting different control locations into the Basic assembler that is an integral part of the program, it can readily be translated for use with other machines having similar data port facilities. Also, the pulse length required for different types of EPROM can be set from the program.

At the end of the listing, the primary control routines of the program are given in Basic, and this section can be used for making initial checks on the unit following assembly. It is recommended that this checking facility is used prior to putting the unit into active service. Once operation from Basic is known to be satisfactory, then make use of the machine code routines. Note though that when checking it is best to only program a few bits at a time, into consecutive sequences, to minimise

Fig.3. *PCB details of the Eprom Programmer*

EPROM PROGRAMMER

```
100 PRINT"EPROM PROG 277 E249 14FEB87":PRINT:CX$="1-PET" :REM 2-C64 3-BBC
110 PRINT:PRINT"SETTING UP":GOSUB440:REM MAKE CX$ = MACHINE IDENTITY AS ABOVE
120 PRINT"":PRINT:PRINT"**SWITCH OFF POWER**":PRINT:PRINT"1 PROGRAM EPROM"
130 PRINT"2 VIEW EPROM":PRINT:PRINT"3 CHECK PROGRAM":PRINT
140 PRINT"4 ERAZURE CHECK":PRINT:PRINT"5 PROGRAM EPROM FROM BASIC":PRINT
150 PRINT"6 CHECK EPROM FROM BASIC"
160 PRINT:INPUT"WHICH";Z$:Z=VAL(Z$):IFZ<1ORZ>6THEN160
170 PRINT"":PRINT:PRINT:PRINT"SWITCH ON POWER - THEN PRESS ANY KEY":PRINT
180 GETZ$:IFZ$=""THEN180
190 ONZGOTO200,280,250,340,920,920
200 INPUT"EPROM PULSE LENGTH (10 OR 50)";PU:IFPU=10THENPU=8:GOTO220
210 PU=40
220 IFCX$="3-BBC"THENPU=PU*2
230 POKEPL,PU:REM THESE TIMING FACTORS MAY NEED CHANGING - SEE PUBLISHED TEXT
240 GOSUB390:PRINT:PRINT"PROGRAMMING":SYS(SY+54):PRINT:PRINT"END PROGRAMMING"
250 PRINT:PRINT"CHECK EPROM PROG":POKEOUT,4:POKEOUT,0:GOSUB410:SYS(SY+137)
260 A=PEEK(ZZ+1)*256+PEEK(ZZ):IFA=0THENPRINT:PRINT"OK END CHECKING":GOTO360
270 PRINT:PRINT"*** ERROR FROM MEMORY LOCATION "A:GOTO360
280 PRINT:PRINT"VIEW EPROM":POKEOUT,4:POKEOUT,0
290 FORJ=0TO4095:SYS(SY):PRINTJ;PEEK(ZZ+1):GETZ$:IFZ$=""THEN330
300 PRINT:PRINT"HOLDING - [M] MENU  [BAR] CONTINUE"
310 GETZ$:IFZ$=""THEN310
320 IFZ$="M"THEN120
330 NEXT:PRINT:PRINT"FINISHED":GOTO360
340 PRINT:PRINT"CHECK EPROM ERAZURE":SYS(SY+185):A=PEEK(ZZ+1)*256+PEEK(Z)
350 PRINTA" BITS CLEARED"
360 PRINT:PRINT"ANY KEY FOR MENU"
370 GETZ$:IFZ$=""THEN370
380 GOTO120
390 POKEOUT,4:POKEOUT,0:PRINT:INPUT"EPROM START ADDRESS";ES
400 PRINT:INPUT"MEMORY START";MS:PRINT:INPUT"MEMORY END";ME
410 H=INT(ES/256):L=ES-(H*256):POKEMM+4,L:POKEMM+5,H:IFES>0THENSYS(SY+219)
420 H=INT(MS/256):L=MS-(H*256):POKEMM,L:POKEMM+1,H
430 H=INT(ME/256):L=ME-(H*256):POKEMM+2,L:POKEMM+3,H:RETURN
440 ONVAL(CX$)GOTO460,480,510
450 REM PET
460 POKE53,94:POKE52,0:SY=24576:REM SEE NOTE AT VERY END
470 DRT=59459:IN=59457:OUT=59471:DN=205:UP=237:AT=59468:ZZ=0:MM=733:GOTO530
480 REM C64
490 DRT=56579:IN=56577:OUT=IN:DN=251:UP=199:AT=56576:ZZ=251:MM=49408
500 SY=49152:GOTO530
510 REM BBC
520 DRT=&FE62:IN=&FE60:OUT=IN:DN=14:UP=206:AT=&FE6C:ZZ=112:MM=116:SY=3329
530 POKEDRT,127:POKEOUT,0:A=SY-1:A$="":PL=PEEK(MM+15)+SY
540 I$="EPROM277":FORE=MM+7TOMM+14:A$=A$+CHR$(PEEK(B)):NEXT:IFA$=B$THENRETURN
550 FORB=1TO8:POKEMM+6+B,ASC(MID$(B$,B)):NEXT
560 READA$:A=A+1:IFA$<>"A"THENPOKEA,VAL(A$):GOTO560
570 IFLEFT$(A$,1)="Z"THENB=VAL(MID$(A$,2)):POKEA,ZZ+B:GOTO560
580 IFLEFT$(A$,1)="M"THENB=MM+VAL(MID$(A$,2)):GOTO690
590 IFA$="OUT"THENB=OUT:GOTO690
600 IFA$="IN"THENB=IN:GOTO690
610 IFA$="ATN"THENB=AT:GOTO690
620 IFA$="JSR"THENB=SY:GOTO690
630 IFA$="UP"THENPOKEA,UP:GOTO560
640 IFA$="DN"THENPOKEA,DN:GOTO560
650 IFA$="PLS"THENPOKEA,8:PL=A:POKEMM+15,A-SY:GOTO560
660 IFA$="END"THENRETURN
670 PRINT"PROBLEM = ";A$:STOP:REM IF ERROR CHANGE B$ ABOVE TO DIFFERENT NAME
680 REM OTHERWISE NEXT RUNNING WILL BYPASS MEMORY LOADING STAGE
690 M=INT(B/256):L=B-(M*256):POKEA,L:A=A+1:POKEA,M:GOTO560
700 DATA160,0,132,Z1,169,16,141,OUT,140,OUT,162,128,160,8,173,IN,41,128,240
710 DATA5,138,5,Z1,133,Z1,138,24,106,170,169,8,141,OUT,169,0,141,OUT,136,208
720 DATA227,169,64,141,OUT,140,OUT,96,162,4,202,139,M0,149,Z0,224,0,208,246
730 DATA232,160,0,138,49,Z0,240,1,200,208,Z0,165,Z1,197,ATN,169,DN,141,ATN
740 DATA133,10,170,208,230,169,34,141,OUT,162,PLS,200,208,253,202,208,250,140
750 DATAOUT,169,64,141,OUT,140,OUT,Z0,Z0,208,2,230,Z1,165,Z1,197,Z3,144,193
760 DATA165,Z0,197,Z2,144,187,96,0,173,M0,133,Z2,173,M1,133,Z2,32,JSR,160,0
770 DATA177,Z2,197,Z1,208,52,230,Z2,208,2,230,Z3,165,Z3,205,M3,144,232,165,Z2
780 DATA205,M2,144,225,169,0,133,Z0,133,Z1,96,160,0,132,Z2,132,Z3,32,JSR,165
790 DATAZ1,101,255,208,10,230,Z2,208,243,230,Z3,201,16,208,237,165,Z2,133,Z0
800 DATA165,Z3,133,Z1,96,162,0,134,Z0,134,Z1,169,64,141,OUT,142,OUT,230,Z0
810 DATA203,2,230,Z1,164,Z1,204,M5,144,237,164,Z0,204,M4,144,230,96,0,0,END
820
830 REM BBC GUIDE LINES
840 REM THE BBC USES '?' IN PLACE OF 'PEEK' AND 'POKE'. THUS 'POKEA,UP'
850 REM BECOMES '?A=UP'. FOR 'PEEK' THE '?' CAN BE SUBSTITUTED DIRECTLY
860 REM THUS 'PEEK(ZZ+1)' BECOMES '?(ZZ+1). 'SYS' BECOMES 'CALL' SO 'SYS(SY)'
870 REM BECOMES 'CALL(SY)'. 'GETZ$' BECOMES 'Z$=INKEY$(0)'. WHEN TYPING IN
880 REM NORMAL BBC REQUIREMENTS FOR A SPACE BETWEEN SOME STATEMENTS MUST BE
890 REM OBSERVED. SYMBOL '' BECOMES 'CLS'
900
910 REM 'BASIC' EQUIV TO PROGRAM EPROM FROM ADDRESS X TO X + Y WITH 0 TO Y
920 INPUT"EPROM START ADDRESS";X
930 INPUT"MAX PROGRAM LENGTH (LESS THAN 256)";Y:IFZ=6THEN1010
940 INPUT"EPROM PULSE LENGTH (10 OR 50)";PU:IFPU<>10THENPU=50
950 IFCX$="3-BBC"THENPU=PU*2
960 REM THESE TIMING FACTORS MAY NEED CHANGING - SEE PUBLISHED TEXT
970 GOSUB1040:FOR A=0 TO Y:PRINT A:FOR B=0 TO 7:K=0:E=2↑B:IF A AND E THEN K=1
980 POKEOUT,K:POKEAT,UP:POKEAT,DN:NEXT B:POKEOUT,34:FOR C=1 TO PU:NEXT
990 POKEOUT,0:POKEOUT,64:POKEOUT,0:NEXT:PRINT:GOTO360
1000 REM 'BASIC' FOR READING BACK
1010 GOSUB1040:FOR A=0 TO Y:POKEOUT,16:POKEOUT,0:B=0:FOR F=7 TO 0 STEP-1
1020 C=PEEK(IN) AND 128:C=ABS(C>0):D=2↑F:B=B OR (D*C):POKEOUT,3:POKEOUT,0:NEXT
1030 PRINTA,B:POKEOUT,0:NEXT:GOTO360
1040 POKEOUT,4:POKEOUT,0:REM RESET
1050 IF X<>0 THEN FOR A=1 TO X:POKEOUT,64:POKEOUT,0:NEXT:REM STEP FORWARD
1060 RETURN
1070 REM NOTE TO PET USERS
1080 REM POKE53,94:POKE52,0:SY=24576' :THESE FIGURES RELATE TO PET MEMORY TOP
1090 REM ALTERNATIVE NUMBERS SHOULD BE ENTERED IF MACHINE IS NOT 32K OR IF
1100 REM OTHER MACHINE CODE ROUTINES ARE ALREADY LOADED. THE NEW NUMBERS ARE
1110 REM FOUND BY RUNNING THIS SHORT ROUTINE
1120 REM A=PEEK(53)-2:POKE53,A:POKE52,0:SY=A*256:PRINTA,SY
1130 REM C64 & BBC USERS NEED NOT WORRY FOR MACHINE CODE IS STORED IN AREAS
1140 REM RESERVED SPECIALLY FOR USERS OWN CODE - THE PET HAS NO SUCH FACILITY.
READY.
```

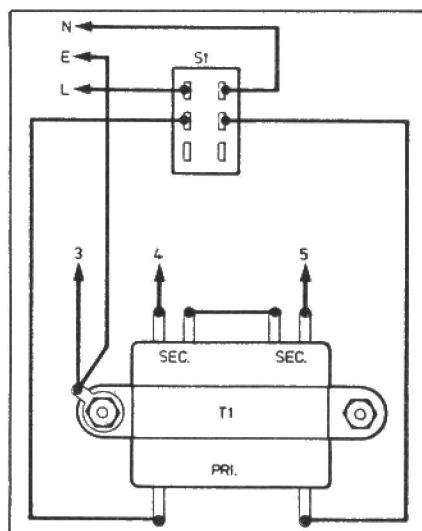**PROGRAM LISTING FOR THE EPROM PROGRAMMER (See Text)**

Fig.4. *Transformer and switching wiring*

PCB Pin 1 – Computer 0V (GND)
PCB Pin 2 – 0V (spare)
PCB Pin 6 – Raw DC+ input (see text)
PCB Pin 7 – Vpp test point
PCB Pin 8 – Raw DC 0V input (see text)
PCB Pins DA0 to DA7, and ATN goto computer socket

ADDITIONAL CONNECTIONS ON PCB

using up EPROM space. The EPROM will of course need erasing before using it fully.

OTHER EPROMS

You are not restricted to using just the TMS2532A, other types can be used as long as their pin configurations are the same, and that the Vpp level and pulse duration are set according to the relevant data sheet requirements.

WELL PAST CHRISTMAS!

Several weeks have passed since putting the unit into operation (but as I write this it's still snowing!), and during this time I have not only relocated 4K of subroutines, but processed several EPROMs for other purposes and friends. In retrospect I don't know why I never made use of an EPROM programmer before, they are remarkably useful, as I am sure you will find should you decide to build this one – which I hope you will. **PE**

Fig.5. *User port connections*

READERS' LETTERS

SATELLITE TV PROSPECTS

Dear PE

In response to your *Leading Edge* article on the above subject in the June issue I feel that I must write to you and clarify certain points that your readers may find misleading.

The first point to note is that Satellite TV is here to stay and Richard Hooper's statement that he does not expect a market before 1995 either tells me that he has not done his market research or he has not read the newspapers. If he is correct please explain why the French and Germans are launching two direct broadcast satellites later this year, why Astra is launching a medium power satellite mid 1988 and why the British Satellite Broadcasting Consortium is spending nine hundred million pounds and launching its DBS satellites in December 1989. All of these satellites are specifically designed for dish owners – not cable systems. Rather than the direct satellite market not taking off before 1995, I suggest that as the hardware cost for individual dish owners is now down to twenty pounds per month (based of a five year payout) it is the cable companies that will start feeling the squeeze as most of them are already charging more than this for a basic connection.

Secondly, while it is true that you can spend up to two thousand pound for a system, it is generally only the enthusiast that will do so. The family owner that wishes to watch satellite TV needs to pay a maximum of seven hundred and fifty pounds for a remote control system (installation and VAT included!) upgradable to a multi-satellite system for an additional four hundred pounds. If he is paying more than this I suggest he looks around.

Third, Andy Birchall's statement that Premiere has to scramble is correct and I for one welcome his statement. Most satellite dealers recognise that without adequate programming there is no need to sell the hardware and without licence fees there will be no programming. Your statement, however, that the cost of decoders will be prohibitive is wrong – initially they will cost just forty pounds! Premiere also plans to move over to the Astra Satellite and the idea behind this is surely to broadcast to domestic dish owners – to charge a "prohibitive" fee for a decoder is surely not on.

Finally, as far as licence fees are concerned it is only fair and right that the consumer pays them – two pounds thirty-six pence per week for a dedicated arts channel, news channel, seven hours of sport a day, one hundred and fifty plus films per month and a monthly TV guide seems good value to me! Even if I do not wish to watch these channels there are still a number of free English language channels and many foreign ones for me to watch.

Bert Bridgman
Finance Director
Dorset Dish Satellite TV Ltd
Parkstone, Dorset

PARALLEL BARS

Dear Sir,

I have particularly appreciated the four or five recent articles dealing with such digital principles as A.D.A. conversion, synthesised frequency generation, signal processing, with the accompanying constructional items. To many of us older readers these articles are invaluable in helping us to catch up and understand the current approaches.

The August article by the Prof was very clear and informative. Towards the end he mentioned polyphonic pianos and I am hoping that in a future article he will reveal the way in which polyphonic frequency generation and wave shaping are accomplished for sixteen parallel channels.

There must be many of us, spurred on in the past by PE, who have built analogue organs of many varieties, and who would welcome a constructional article to enable us to rebuild them using digital techniques. Without such aid, I for one would not have the courage to start.

Keep up the good work.

W.A. Sawyer, Beaconsfield.
How about some digital polyphony Prof? Exercise on parallel bars should keep you well keyed up.
Ed.

ANONYMOUSLY ANXIOUS

One reader, who does not want his letter published, has written in to query my editorial about writing for PE (June 87).

Although it has given him food for thought, he feels that my reference to authors supplying PCB track masters, and using CAD systems, is tantamount to putting our projects beyond the reach of interested amateurs. He agrees that PE should be educational and up to date in the feature articles, but wants the constructional articles to be within the reach of ordinary mortals. He believes that there is nothing to be lost by repeating earlier ideas, perhaps with more modern components or techniques, for the benefit of the next generation of amateurs, but wants us to keep the difficulty and cost down. Additionally, he says that the quality conditions placed on the submission of drawings and texts almost prohibits amateur authors from submitting papers for publication.

I welcome constructive criticism of PE as much as I appreciate praise from the many readers who think we are an excellent magazine. Only through a good variety of views can we know that we are offering people what they want.

It is not clear though, why my comments on PCB track masters and CAD drawings should have been taken as inappropriate to amateurs. The intention of publishing projects with PCB layouts is to simplify their construction, enabling more readers to reap the benefits and pleasures of the projects. Since PCBs are available through the PE PCB Service and through some advertisers, the assembly will inherently be more straightforward than if readers have to design their own layout, even though that can be interesting in its own right. As far as the authors are concerned, the design of a PCB layout for publication is not difficult, and should be within the capabilities of anyone who has sufficient electronics knowledge to have a project design accepted for publication. The availablity of suitable drafting materials is no problem since there are new sources.

The CAD reference was not a statement that authors should use CAD, rather, that those who already possess or have access to such systems should feel free to use them for their articles and projects. If an author can only supply drawings done by hand, his or her work will just as readily be considered for publication. All that I ask is that hand drawn diagrams should be neat enough for our art department to be able to read them and produce their own artwork. Script-wise though I must insist on typed texts or computer printouts for all but the shortest of contributions. Hand written scripts are notoriously prone to being illegible, and our typesetters prefer to attain accuracy at the first setting!

I agree with him that there is a role for selectively repeating earlier ideas in an updated form. While we wish to offer information about new technology and its benefits, we are also conscious of meeting the needs of newcomers to electronics. Some ideas are useful and interesting irrespective of era, and can be re-presented every once in a while, but using current techniques to achieve the desired function.

PE intends to maintain a balance between simplicity and complexity, hi-tech and everyday-tech, and continue to encourage interest in a fascinating subject. It has many aspects and through our authors, both professional and amateur, we wish to show you a reasonable cross-section.
Ed.

TYPL SETLING ARRERS

Dear Ed,

Referring to the letter from J. Duffill (Aug 87), I wish to say that I don't find the captions at all irritating, but neither are they as amusing as some of the inspired typesetting misprints, including such gems as 'trickly charging' and 'improved biasing with tipple rejection'.

The only truly irritating feature of the magazine is the steadfast refusal of some authors (notably the Prof) to put arrows on their block diagrams, so that I get lost in a maze of unlabelled feedback loops.

T.F. Jones, Stockport.
Almost 'That's Life' award material! We are asking the typesetters to check the liquid contents of their font, and the Prof to refletch his amazing quill.
Ed.

IF YOU HAVE ANY COMMENTS, CRITICISMS OR SUGGESTIONS, WRITE AND LET US KNOW. WE ARE INTERESTED IN WHAT YOU THINK AND SAY.
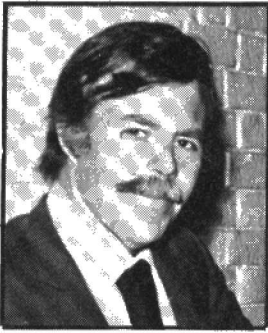
INDUSTRY NOTEBOOK

ELECTRONICS IN MODERN DEMOCRACY

**REPORT BY
TOM IVALL**

We have the technology to fully bring power to the people, but is such democracy really what we want, or what we need?

DURING the General Election earlier this year I wouldn't be surprised if a few readers of PE were triggered into thinking a bit about the Representation of the People (as the relevant Act is called) and wondering whether electronics has had any effect on this political process we call democracy.

Clearly, television was highly effective in presenting the politicians, their personalities and electioneering activities, in a vivid way which could not have been matched by any other medium. But I don't think it helped anybody to think very clearly about the issues. You remembered the facial expressions, the tones of voice and body language but you didn't recall much of what the protagonists actually paid. Television certainly shows the busy surface phenomena of electioneering and may have helped some politicians to persuade the voters one way or another, but I doubt if it is a fundamental influence in political decision-making.

Much more significant, to my mind, is the interaction of computer technology with the processes of government. Because our governments are brought in by democratic elections this interaction also has a bearing on the processes of representative democracy. Industrialised countries like Britain are run by large, loosely-interlocking organizations. Of these the most powerful are the government ministries operated by civil servants. The others are semi-governmental bodies like national research laboratories and state-owned industries. All these organisations rely on information to make decisions which affect the way the country is run. And nowadays this information is increasingly being stored and processed in computer systems, often linked together by data communication networks.

So we have a considerable amount of computer equipment controlled by a relatively small number of officials. It is a powerful assembly of hardware, software and specialised information with experts in charge. On the other hand, it is not all-powerful. A strike by computer staff can suddenly halt at least a part of it and throw the organisation concerned into confusion.

In a democracy you might expect all this technical apparatus to be somehow under the control of the people, at least indirectly, through their representatives in Parliament. So it is — theoretically. But in practice the control is so indirect and tenuous as to be almost non-existent. The will of the people seems to count for less and less as the officials in charge of the specialised information and of the systems handling it become increasingly influential in political decision-making.

In many countries the power of legislative assemblies like our Parliament has been declining relative to the power of the executive. This has happened because of the increasingly technical decisions which a modern government has to make. Such decisions are often beyond the competence of the ordinary representative of the people like MPs, so they have to be made under the guidance of the technical experts in the permanent bureaucracy of the executive — our civil servants, for example.

These bureaucrats always have better, more specialised information at their command than the legislators, and they keep it to themselves when it suits their purposes. The Irangate business in the USA just shows what unelected officials can get up to.

The guidance given by specialist officials increasingly takes the form of the already prepared decision. This decision is the logical outcome of some technical conclusion or necessity which the legislators can't reasonably refuse to endorse. It's difficult for mere members of the public to contest the specialists' arguments because, without full information, the truth of the premises can't be examined.

Information technology has become something like the nervous system of the human body. Without their computer and data transmission systems the officials would now fail to keep control of their organisations. At the same time the very presence of such systems allows the organisations to grow larger and larger, in terms of the resources and people they command, without danger of falling apart. They are integrated and secure. And the heads of these power structures — not elected by the people but using the technical products of their work — make virtually secret decisions which can have profound effects on the way the whole country is governed.

One way in which this dangerous imbalance of political power might be corrected is by the very technology that supports the power structures. I seem to remember that one of the fringe political parties in the recent General Election was recommending electronic voting for day-to-day democratic decision-making. Presumably this would be a way of speeding up a national referendum on a particular issue. Through data terminals attached to domestic telephones we now have the basis of the technology to put it into effect.

The idea might work well for certain big national issues — say the question of capital punishment — where the collective wisdom and will of the public doesn't depend on a mass of detailed, highly specialised information. Taken to its logical conclusion, however, this principle would mean that our present system of Parliament and government would become redundant. Some might say this would be a good thing. But in practice I think we are all really quite glad to hand over the difficult business of running the country to a bunch of people who have offered to do it for us.

On the other hand, there might be a case for rather more involvement of the public in direct decision-making than is typical of a national referendum. Here, the people would have to be given all the specialized information relevant to each issue that required a vote.

Again, we do have the technology to make it possible — the interactive terminal connected through the telephone or cable TV system to a distant computer or database. Examples in the UK are the Prestel viewdata service and schemes like electronic home shopping and banking. The user can call up required information from the database and display it on a monitor screen or printer. He/she then makes an appropriate decision by typing on the keyboard.

But whether our secretive bureaucracy would co-operate in this undermining of their powers is entirely another matter!

BACK NUMBERS, COPIES AND BINDERS

BOOKMARK

The following books have recently been sent to us:

Practical Design of Digital Circuits. Ian Kampel. Newnes Technical Books. £12.50. This book will help the reader with no previous knowledge of digital electronics in the practical aspects of digital design, only familiarity with basic electronic principles being assumed. The book should appeal particularly to engineers and enthusiasts wishing to expand their knowledge in practical rather than theoretical directions.

Batteries for Cordless Appliances. Ralph J. Brodd. Research Studies Press. £24.95. Describes the construction, applicability, operation, characteristics and capabilities of batteries for a wide range of cordless appliances. The book covers buoys and beacons in costal waters; search and rescue beacon equipment; lamps, torches and flashlights, including those of specialised construction, for example on meteorological balloons; scientific apparatus such as oscilloscopes and portable tape recorders, and battery operated toys.

25 Fun-to-Build Projects for Learning Electronics Theory. Tab Books. £6.35. This is a collection of projects that should make learning electronics theory incredibly easy and enjoyable. With its hands-on, here's how it's done approach, even the most elusive concepts of electronics and electricity can become easy to understand and apply. A good book of projects for the beginning hobbyist and a supplementary text for school courses, though it should be noted that it was first published in the USA.

Computer Graphics – A Programming Approach. Steven Harrington. McGraw-Hill. £23.95. This second edition of an introductory text on interactive computer graphics, presents the basic concepts of that field. It encourages a learn-by-doing attitude and provides guidance for developing a graphics system. It also includes suggestions for modifications and extension of the system, and gives relevent application problems.

Microprocessors and Interfacing – Programming and Hardware. Douglas V. Hall. McGraw-Hill. £12.95. For the most part this book is based on a three-quarter series of microprocessor courses taught by the author and his colleagues. It is intended for students in electrical engineering technician training programs, and for people working in industry who want to upgrade their knowledge of microprocessors.

Transistor Selector Guide. J.C.J. Ven. Babani. £4.95. Prepared using the latest computerised techniques, from a vast database of electronic component specifications, this unique guide offers a range of selection tables compiled so as to be of maximum use to all electronics engineers, designers and hobbyists.

POINTS ARISING

SCOPE STORE (JUL 87)
Page 38 Fig.3; Polarity of D3 and D4 should be reversed. C12 should go to junction of D1 and D2 – cut track from C12 to D1 then hardwire it to correct point. Page 41 parts list: C9 and C10 should read 100μF 16V electrolytic. Omitted C11 is 100p ceramic plate.

INFRA-RED TRANSCEIVERS (JUN 87)
Fig.3, page 43, R7 goes to pin 11 of IC2.

POLYWHATSIT PART TWO (JUN 87)
Fig.2 page 35 – IC18 pin 1 goes to 0V. IC18 pin 9 goes to pins 9 of IC10-IC12. The PCB is correct. There are minor apparent differences between the switch wiring in Fig.2 and Fig.5; Fig.5 is correct. These corrections do not affect the correct functioning of the unit.

ZX SPECTRUM I/0 PORT (JUN 87)
IC3A and IC3B symbols should be OR gate symbols.

FIBRE-OPTIC DATA LINK PART TWO (OCT 86)
The opening line should read: "TR3 is the phototransistor, and it is given a small forward bias by R9."

PROMENADER (DEC 86 to Feb 87)
The capacitor across R9 on the PCB is C19 at 10μ 16V. C10 is 10μ 16V. R21 is 4k7. R26 is 10K.

PLUGGING POWER

THERE have been problems in some office buildings in the United States where extensive use of modern electrical and electronic equipment has overloaded the electrical conductors and delta-star transformers. It has also caused damage to electric motors. Although there are no such cases reported in the United Kingdom, there are two contributory factors which could lead to similar situations occurring here.

Whilst individual 13A sockets can deliver 13A, building wiring may be rated so that the average load which can be carried is only 0.5A per socket. This can occur in buildings no more than 10 or 20 years old.

Modern electronic equipment frequently has peculiar load characteristics such that the current in the neutral conductor of a three phase supply feeding individual single phase 240V loads can greatly exceed the current in any one phase conductor.

These same load characteristics can also cause increased current to flow in parts of motors and transformers.

Where office premises are making extensive use of electrical/electronic office equipment it is advisable to have the load currents, particularly the neutral current, checked by a chartered electrical engineer.

From a statement issued by BEITA, The Business Equipment and Information Technology Association. Nothing should ever be taken for granted.

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|		
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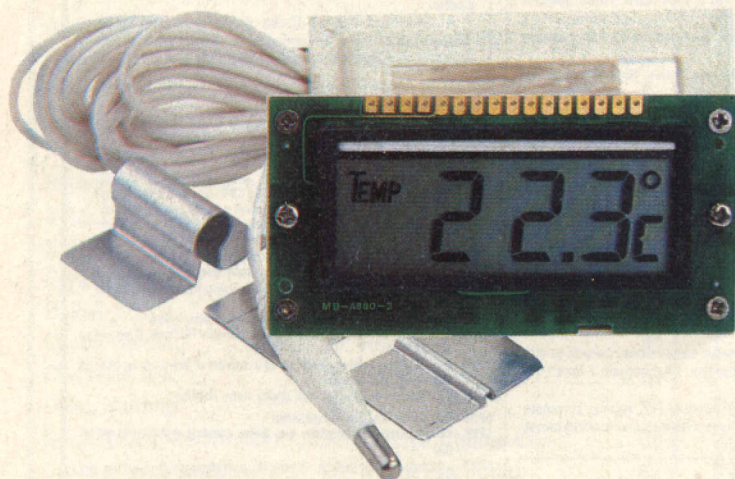
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